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Imaging Failures in Sub-Micron Devices and Measuring Stresses in 3D ICs

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Imaging Failures in Sub-Micron Devices

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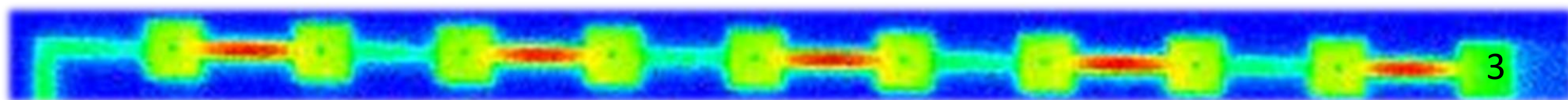
Today's Advanced Devices

- Shrinking device features: 10s nm – 100s um
- More complex circuit architectures
- 3-D Structures
- Higher power densities
- High speed response due to the small thermal mass
- Highly non-uniform

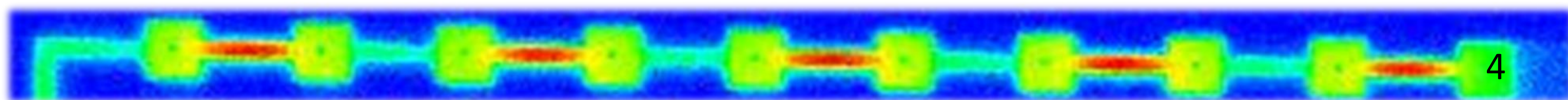


Understanding Device Thermal Behavior

- More important now for …
  - Optimizing device performance and ensuring …
  - Long-term reliability

- Traditional* thermal imaging techniques do not meet requirements:
  - Require sub-micron spatial resolution …
  - Nanosecond time resolution and …
  - Good temperature resolution

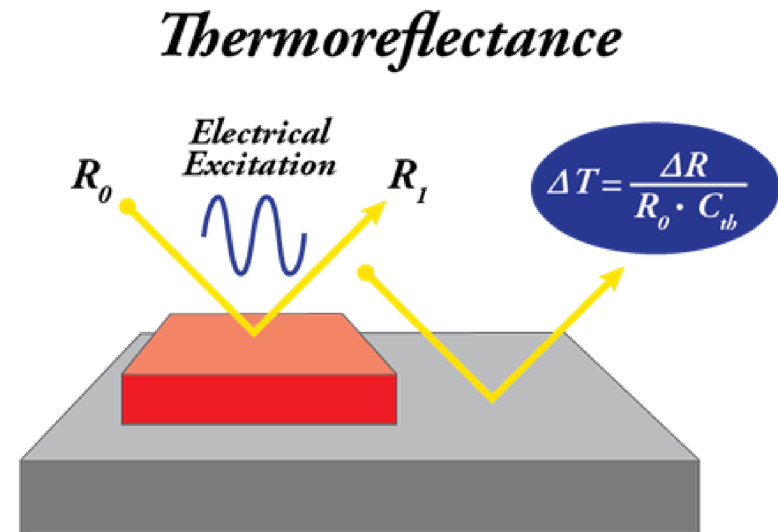
*IR Thermography, Liquid Crystal, Micro-Thermocouple, etc



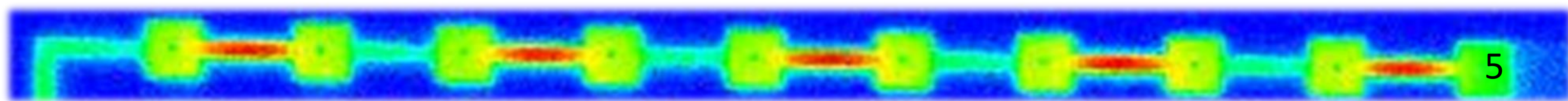
Imaging Based on Thermoreflectance Principle

- Reflectance changes with material temperature
- Non-invasive thermal imaging technique exploits this …

$$\frac{\Delta R}{R} = \left(\frac{1}{R}\frac{\partial R}{\partial T}\right)\Delta T = \kappa \Delta T,$$

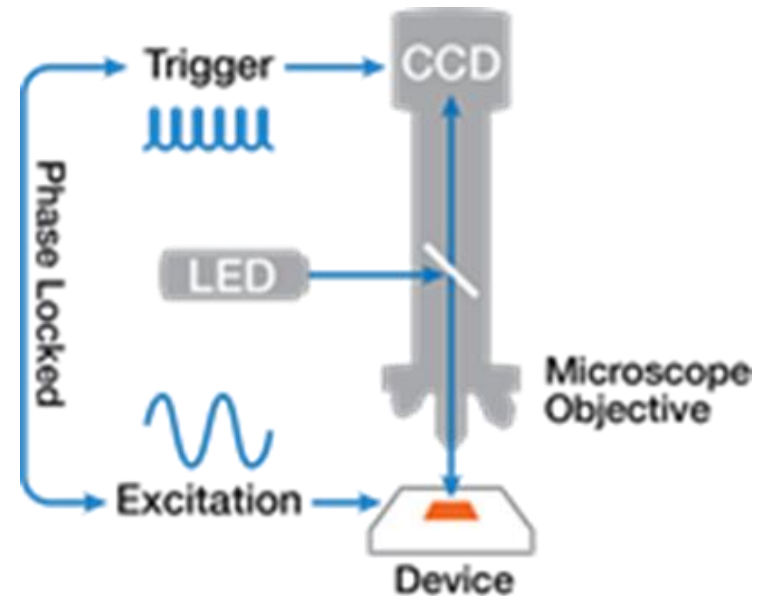


where ***κ*** is the ***Thermoreflectance Coefficient***



Basic Setup for Imaging

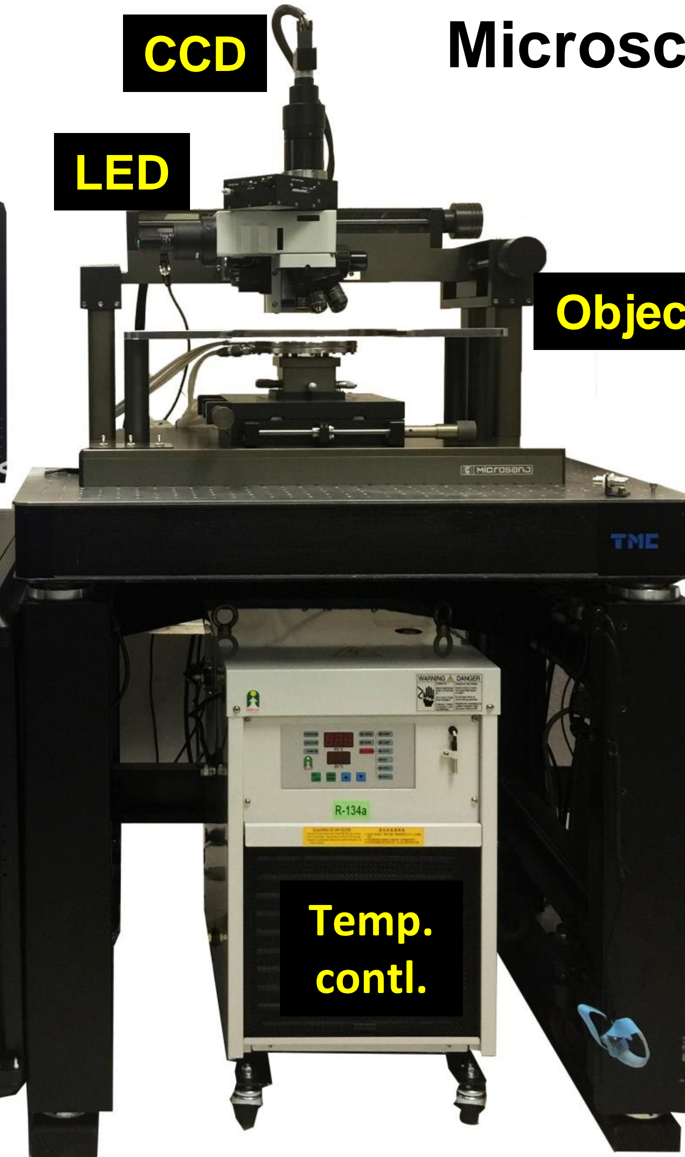
- LED illumination in visible range
- Lock-in technique to enhance S/N ratio
- Thermoreflectance coefficient, κ, is dependent on:
  - Material
  - LED wavelength
  - Relatively independent of ambient temperature

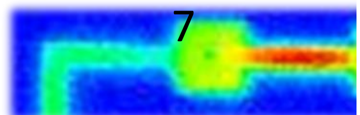


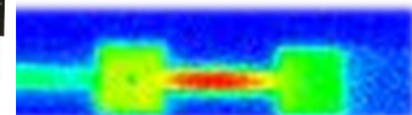
Thermoreflectance Imaging System

Microsanj NT220 Rack

Microscope setup

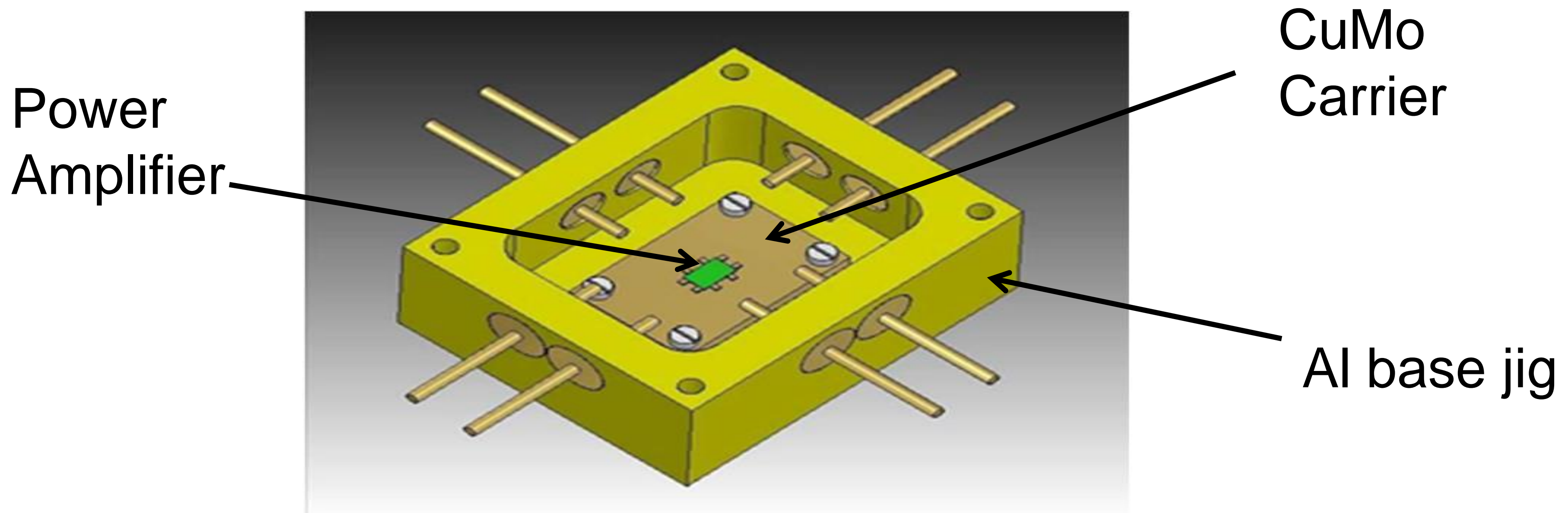






Measurement of Gate Temperature of MMIC Device

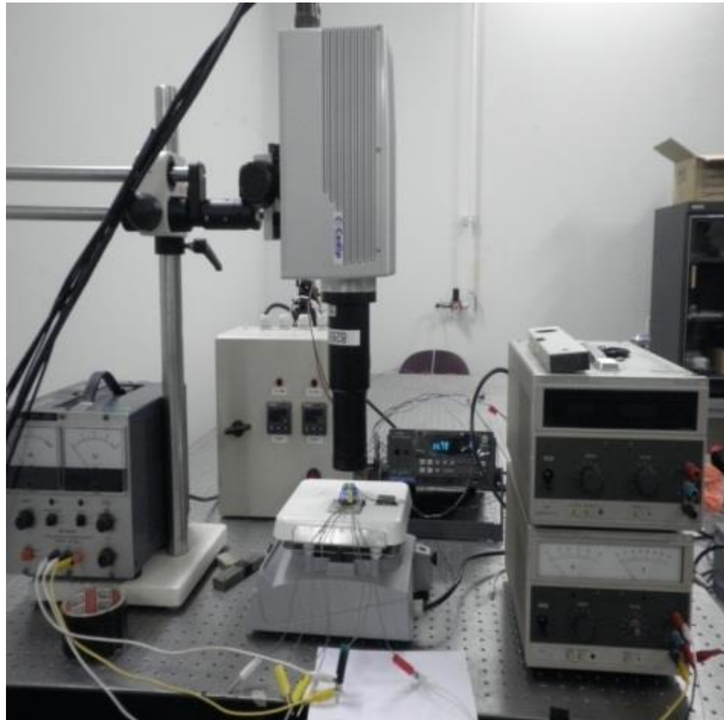
- A GaN power amplifier MMIC device consisting of two gates.
- Length, L_g=0.25μm, Width, W_g=150μm, Pitch, P_g=48μm

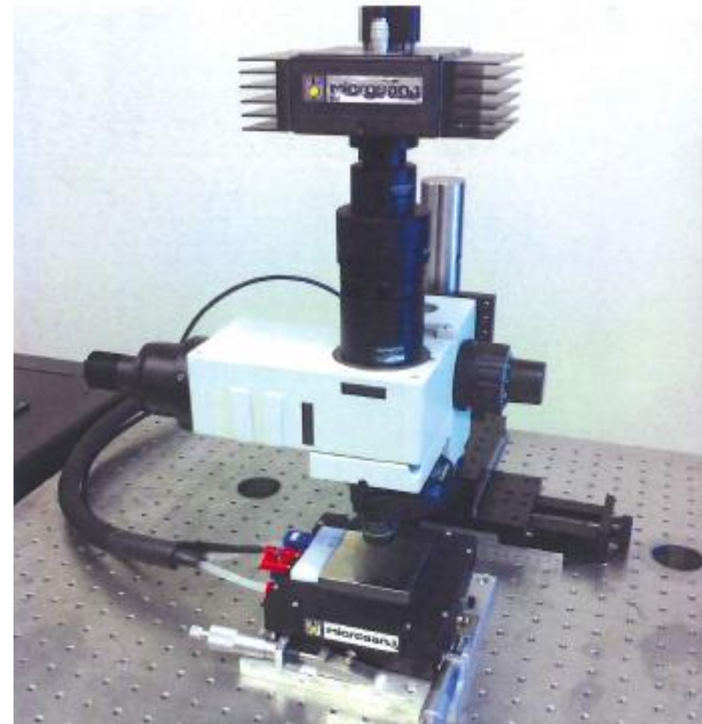


Characterization Techniques

Infrared (IRT)

Thermoreflectance (TTI)





Characteristics of Techniques

NUS National University of Singapore

Infrared (IRT)	Thermoreflectance (TTI)
• Based on blackbody radiation.	• Based on change of reflectivity as a function of change in temperature.
• Emissivity calibration over the surface	• Characterization of material for thermoreflectance coefficient.
• Spatial resolution = 5µm.	• Spatial resolution = 0.300µm (with 100x objective lens)

Thermoreflectance Temperature Measurement

NUS National University of Singapore

20x Res = 0.58 μm

NC2F150Y– THM

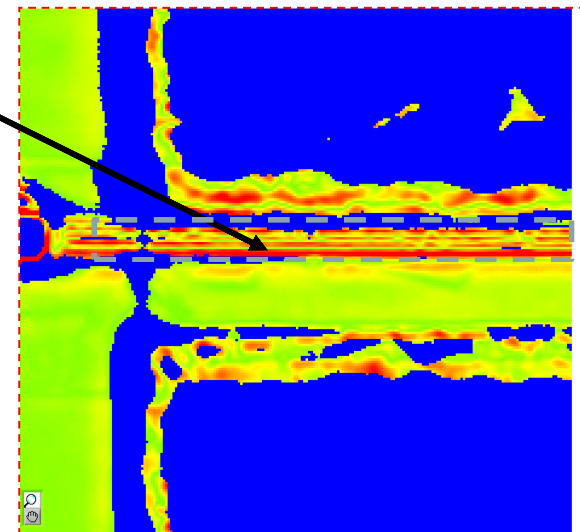
100x Res = 0.3 μm

100x

35.7C

-64.6C

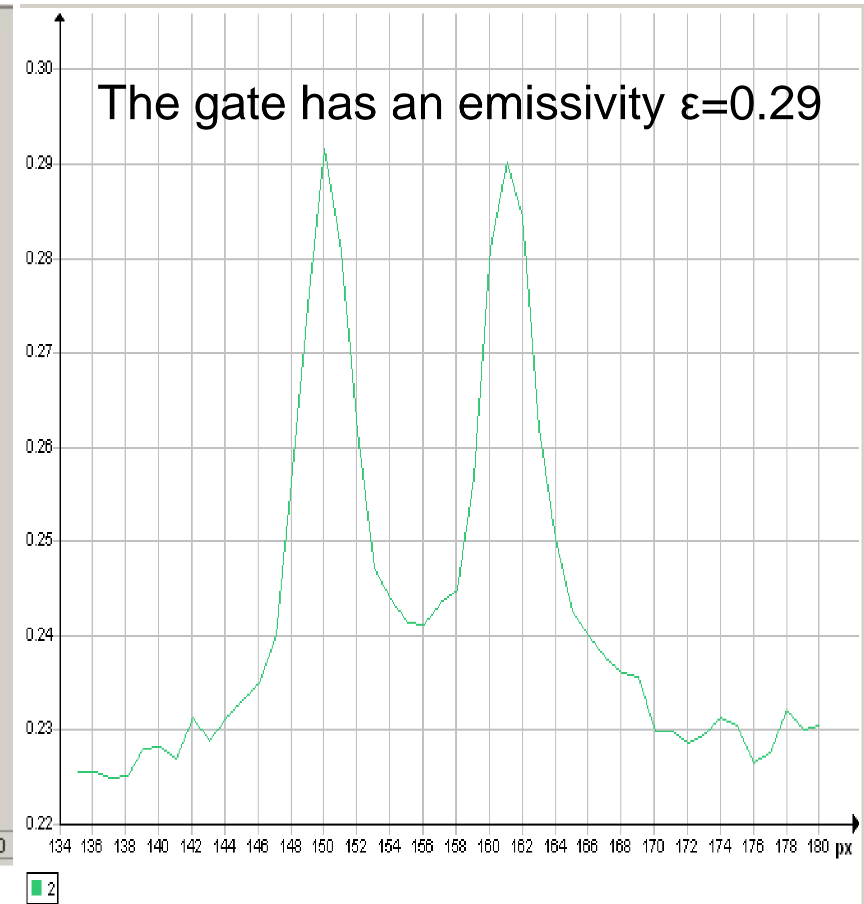
gate



- Only the gates are characterized for κ.
- Therefore, the temperature in regions around the gate is unknown.
- Temperatures around the gates (dark blue regions) are removed to show clearly the heating of the gates of length 0.25 um.
- The red color region indicated in the bottom picture corresponds to where the gate resides.

Emissivity Correction for IRT

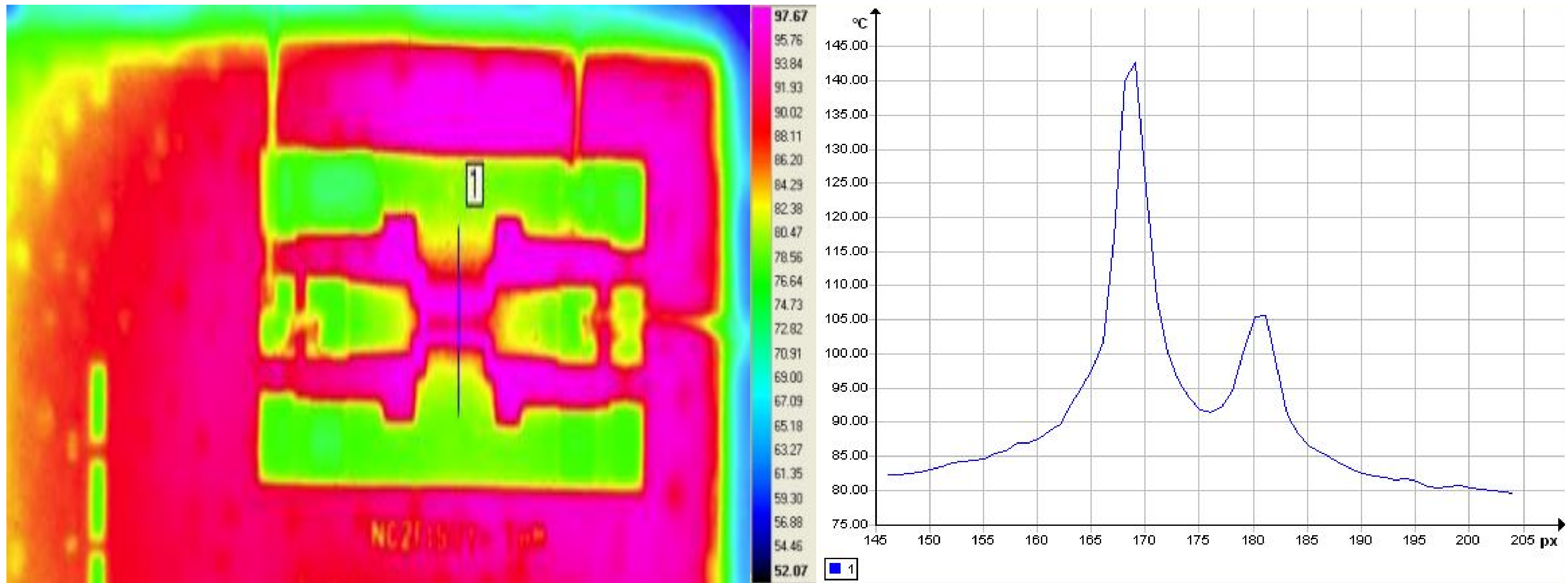
Emissivity Map



Variation of ε along green line

J.H.L. Ling, A.A.O. Tay and K.F. Choo

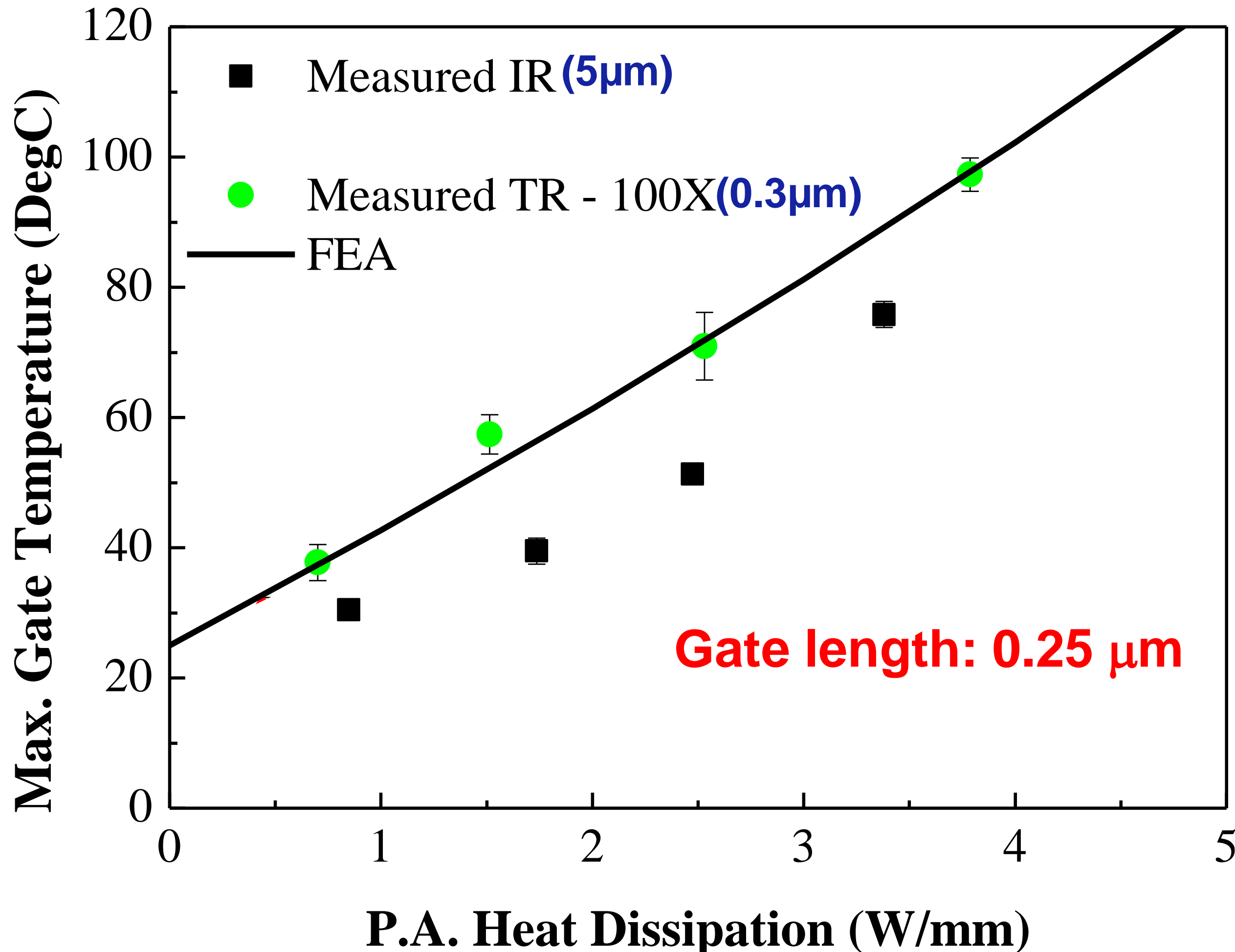
Corrected IR Temperature Distribution



J.H.L. Ling, A.A.O. Tay and K.F. Choo

Comparison of IRT, TTI and FEA

Aluminium jig base temperature of 25°C



Note importance of *spatial resolution* in accurate measurement of gate temperature.

Failure Analysis via Thermal Imaging

- Defects in devices often cause hot spots
- Transient thermal imaging can be used to detect hot spots and hence establish location of defects.
- Thermal behaviour of devices can also give clues to type of defects and failures.

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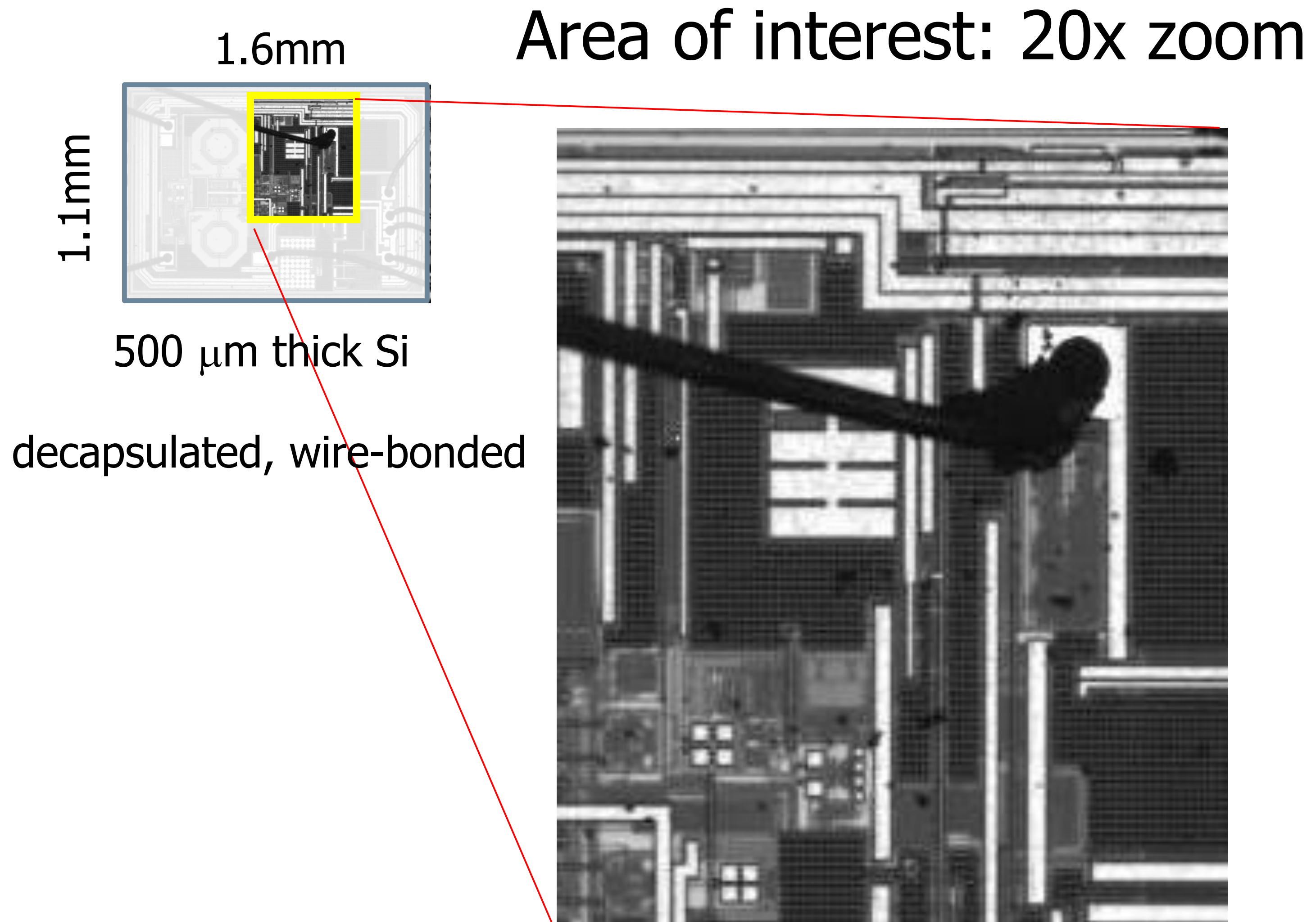
Transient Thermal Analysis of Logic IC



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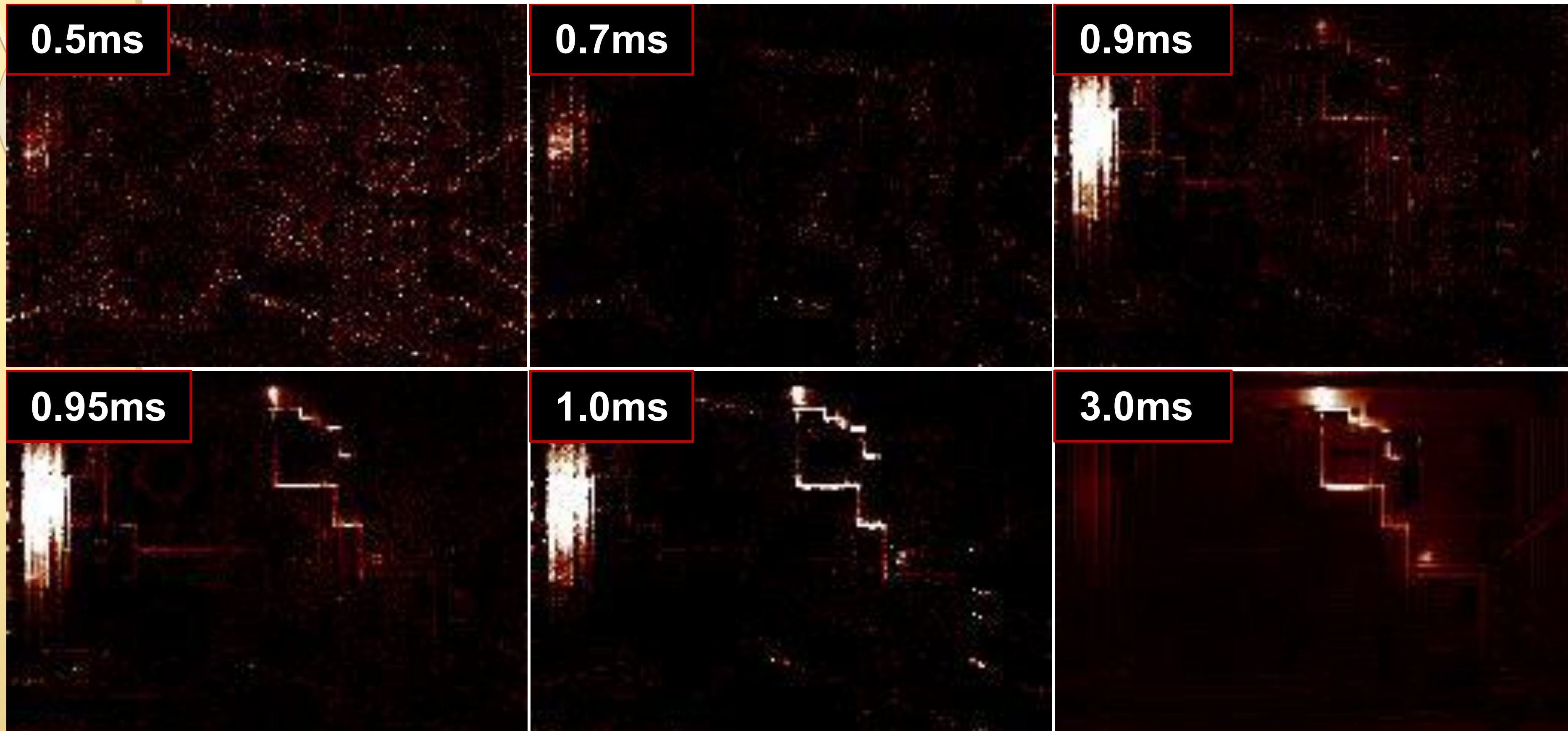
Heating history



A series of thermal intensity contour maps versus elapsed time after applied bias. The brighter location indicates the higher temperature.
The temperature scale is common for all six images. Note that the right side top portion heats up quickly after approximately 1 ms.

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Logic IC - local heat up

Logic sections located at the lower right undergo *latchup* where 250 mA of current flowed through V_{dd} rather than the typical 10 mA.

This large current causes the power path to heat up → visible in the image.

Location of Latchup

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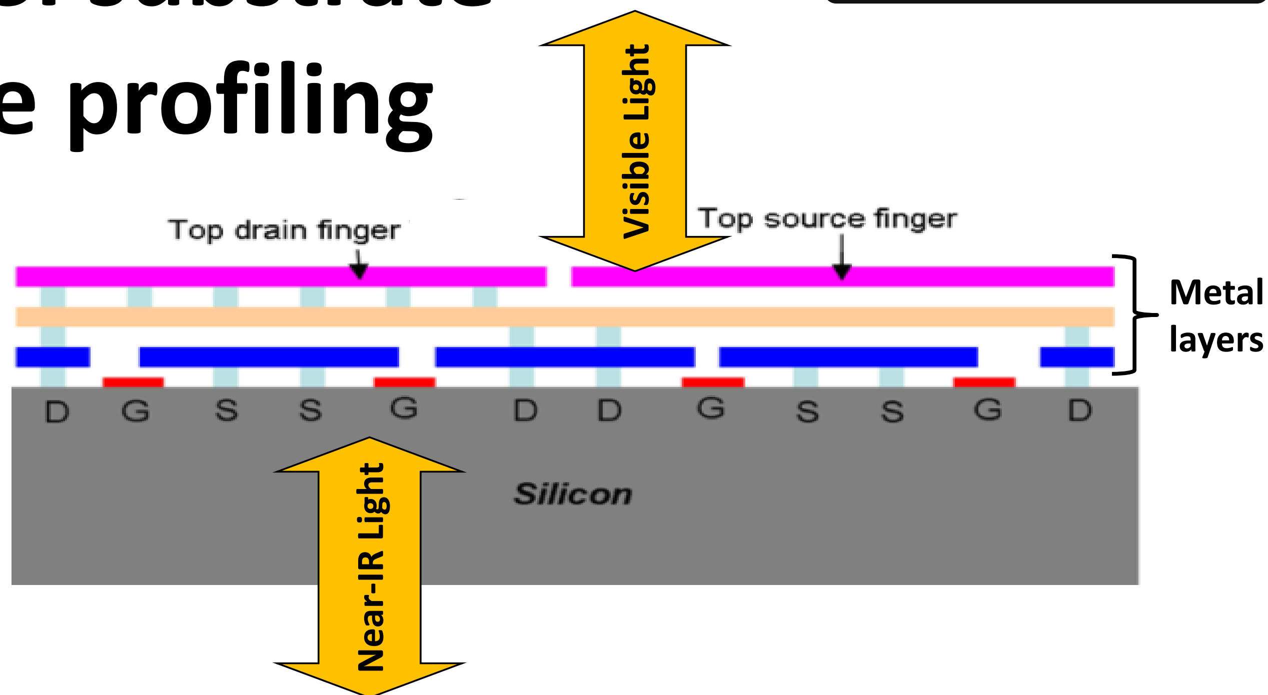
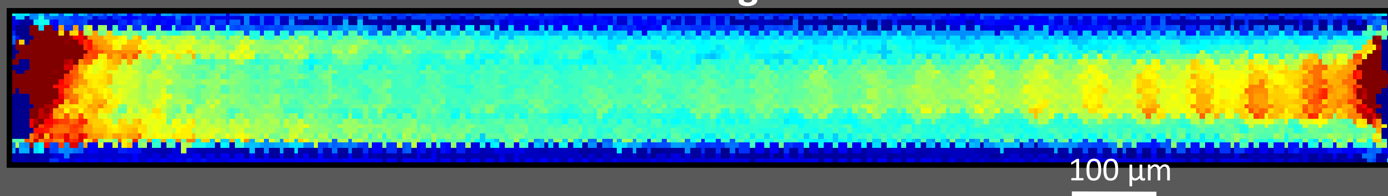
Through the Si substrate temperature profiling

Cross sectional view of LDMOS transistor array



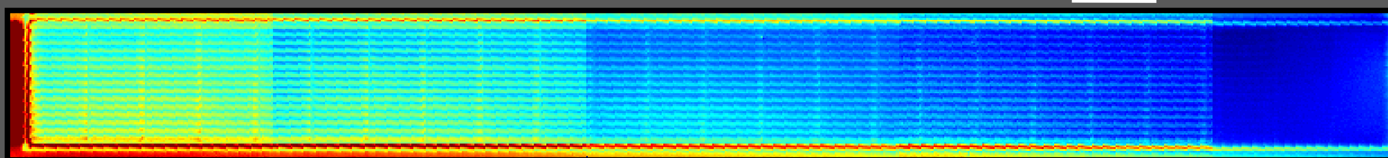
Thermal images

Topside (Si CCD)



6X

Backside (InGaAs CCD)



drain contact

source contact

Thermal Characterization via TTI

- Thermal resistance, $R_{th} = t/kA$ where t is the layer thickness, k is thermal conductivity, A is the area.
- TTI can be used to characterize k, if t is known.
- TTI can be used to measure t, if k is known. This can be used as a way of monitoring manufacturing quality in a non-destructive manner.

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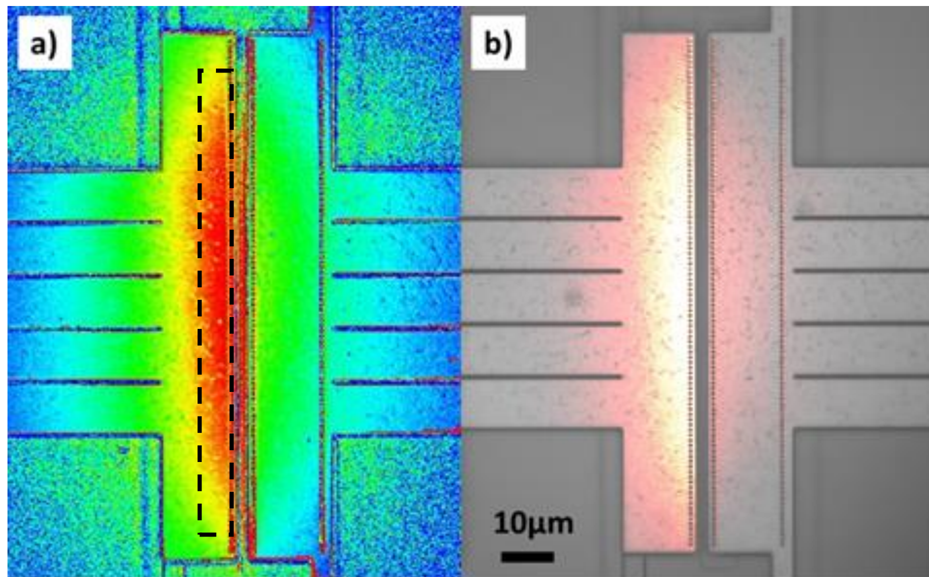
Transient Analysis of a Power Diode

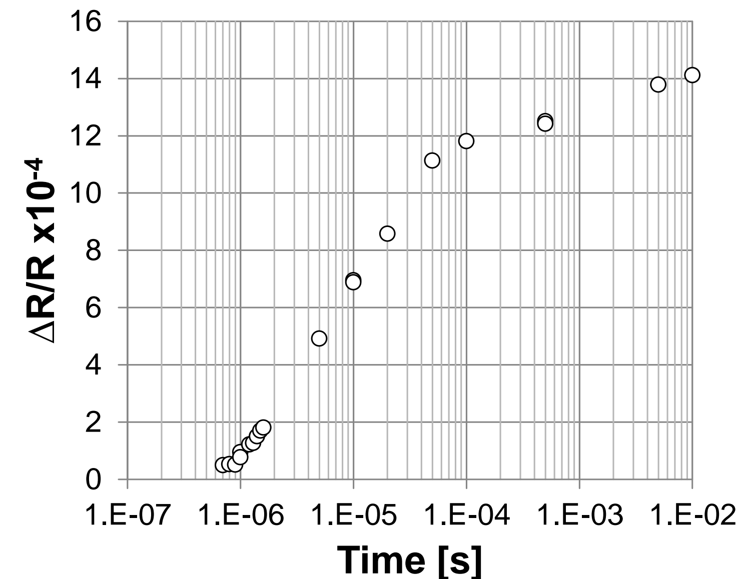
Device image and thermal contour



At 1 ms after step pulse started (715 mA).

- Higher temperature in anode (left) due to accumulation of charged carriers.

Mean temperature response at the marked location of the left contact (anode).



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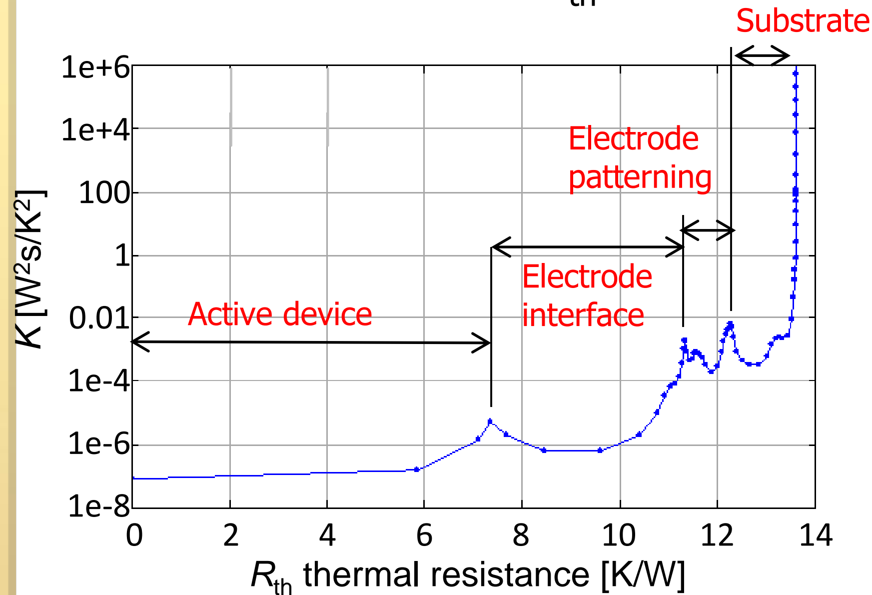
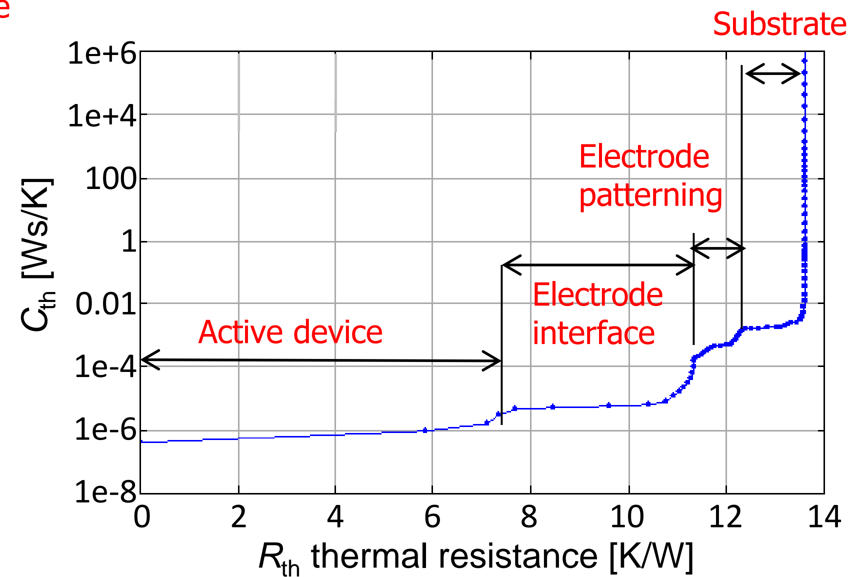
Use Structure Functions to obtain R_{th}

Thermal network analysis by using the structure function method.

Differential structure function K vs Thermal resistance R_{th}.



Cumulative structure function C_{th} vs Thermal resistance R_{th}.



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Conclusion

- Thermoreflectance thermal imaging (TTI) has high spatial resolution (< 300 nm), high temporal resolution (800 ps), high temperature resolution (0.1 ^{o}C).
- TTI is more accurate than IRT for imaging devices mainly due to >10X higher spatial resolution.
- TTI can be used for imaging and analyzing the rapid transient thermal behavior of devices including hot spots which indicate locations of device failure.
- TTI can be used to measure flip chip transistor temperatures by using NIR light through the Si substrate of flip chips.
- *TTI meets the challenging requirements for thermal analysis of today's advanced devices.*

Measuring Stresses in TSVs of 3D IC Packages

Arief Budiman and Andrew A. O. Tay

Singapore University of Technology and Design

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Measurement of stresses in Cu and Si around through-silicon via (TSV) by synchrotron X-ray micro-diffraction for 3-dimensional integrated circuits

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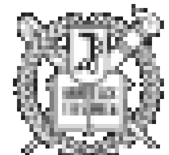
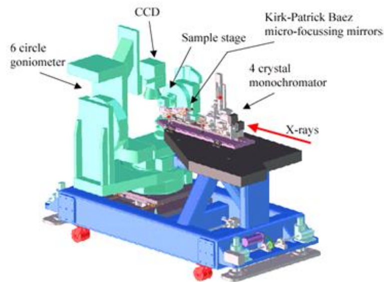
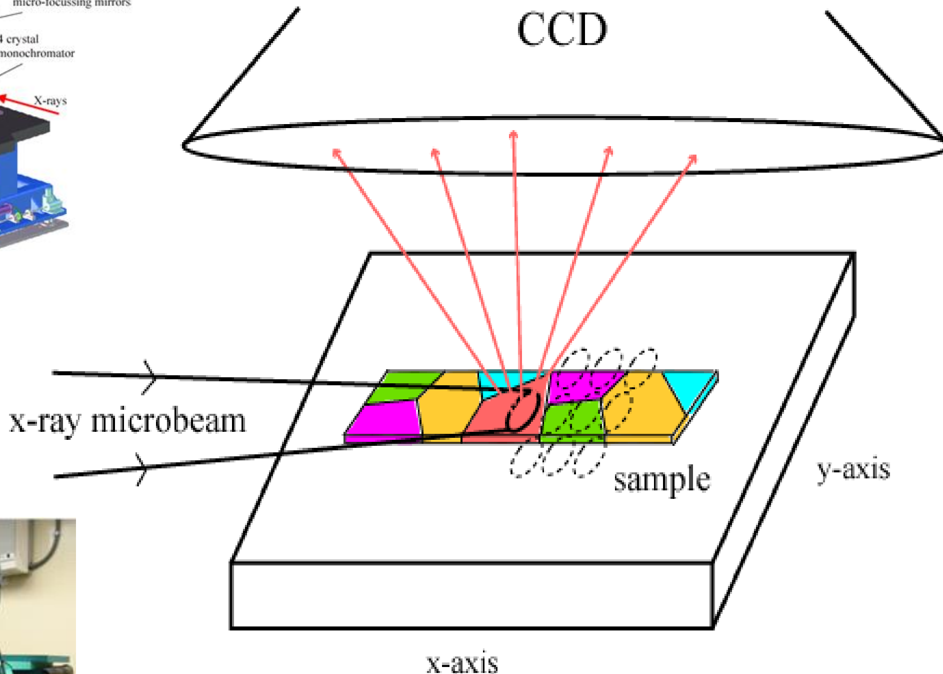
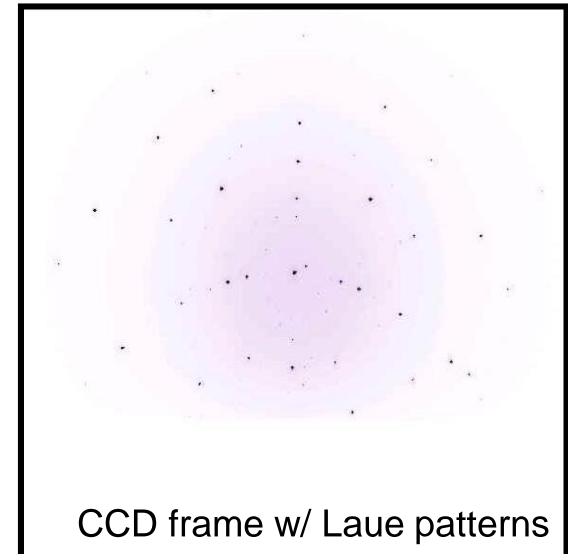


Synchrotron X-Ray Submicron Diffraction

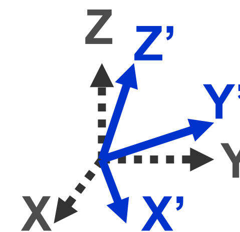


Beam size: 0.5x0.5 μm



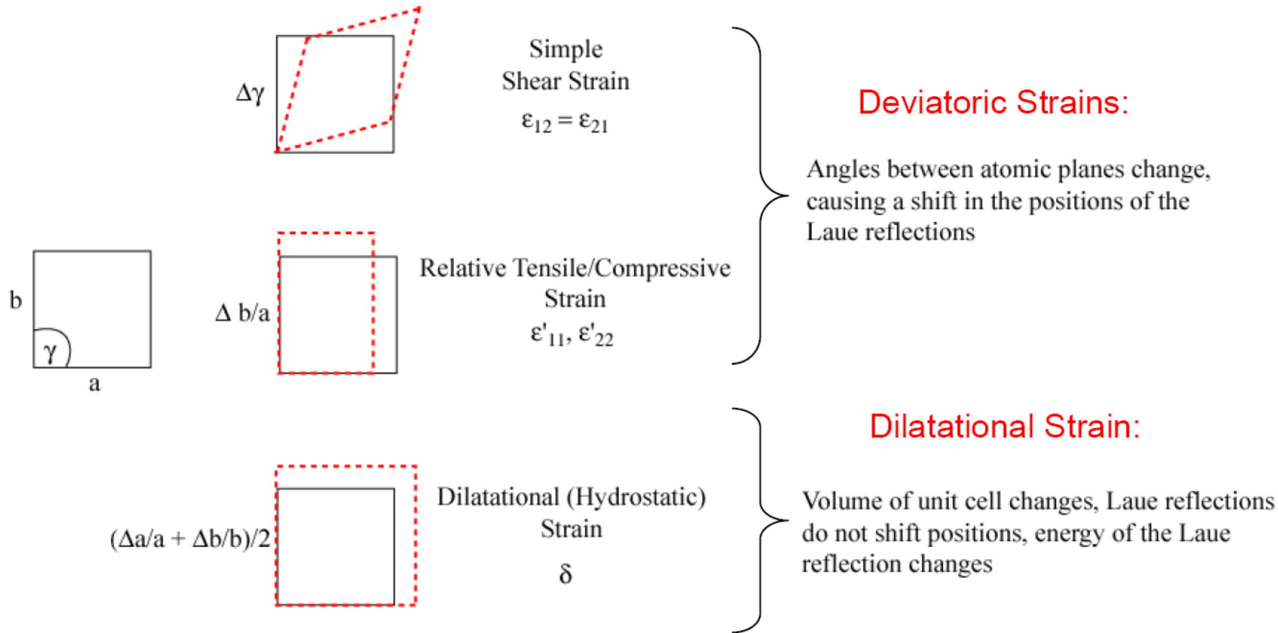


X-ray source: ALS Synchrotron, Berkeley Lab (Beamline 12.3.2)



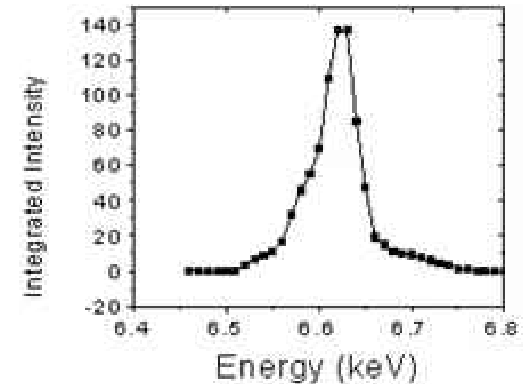
Deviatoric strain tensor: Small shifts in spot relative positions ➔ Crystal deformation at constant volume (~ 10^{-4} accuracy)

Laue pattern and energy scanning



Laue pattern

Energy scanning



Total strain = dilatational + deviatoric

(Energy scan) + (Laue pattern)

$$\varepsilon_{ij} = \begin{pmatrix} \delta & 0 & 0 \\ 0 & \delta & 0 \\ 0 & 0 & \delta \end{pmatrix} + \begin{pmatrix} \varepsilon'_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{21} & \varepsilon'_{22} & \varepsilon_{23} \\ \varepsilon_{31} & \varepsilon_{32} & \varepsilon'_{33} \end{pmatrix}$$

Determination of Complete Strain Tensor

Lab XRD vs Synchrotron μXRD

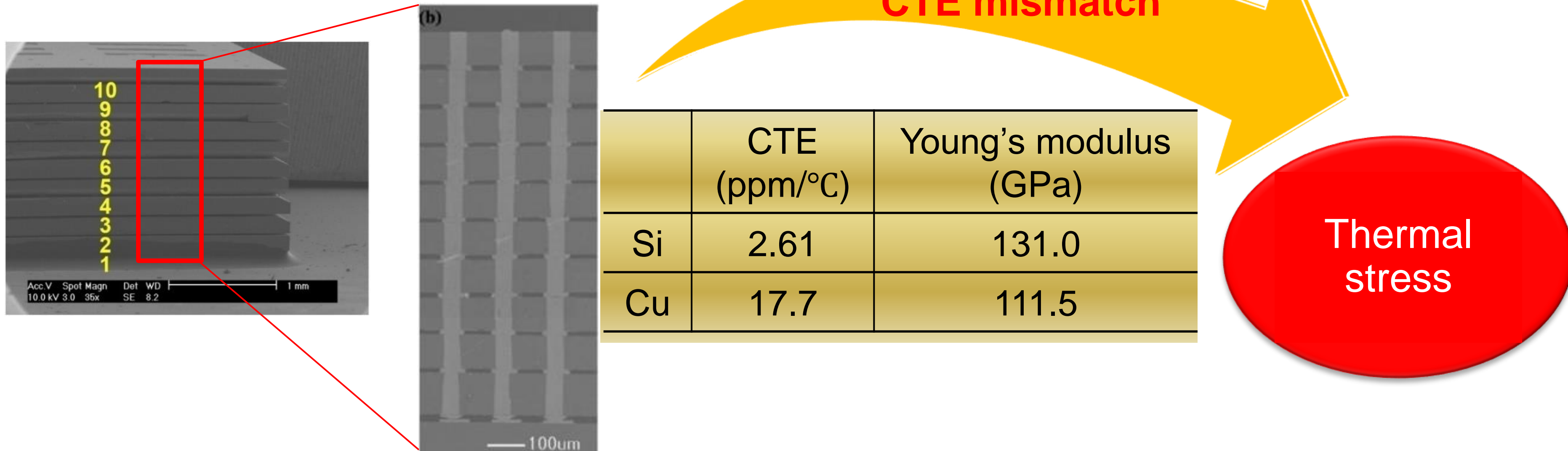
Laboratory XRD usually cannot be used for measuring stress in small TSVs as it has a resolution of about 70 μm which is inadequate.

TSV dia. 20 μm

Diameter 70 μm.

The resolution of a Synchrotron μXRD is 0.5 μm which is very adequate.

Mechanical Stresses in TSV structure



	CTE (ppm/℃)	Young's modulus (GPa)
Si	2.61	131.0
Cu	17.7	111.5

- Cu TSV is embedded in Si matrix.
- Coefficient of thermal expansion (CTE) mismatch → *thermal stress*.
- Thermal stress can be induced during manufacturing or processing.
- Other origins of stress may include *grain growth, chip-package interaction, wafer thinning, etc*.

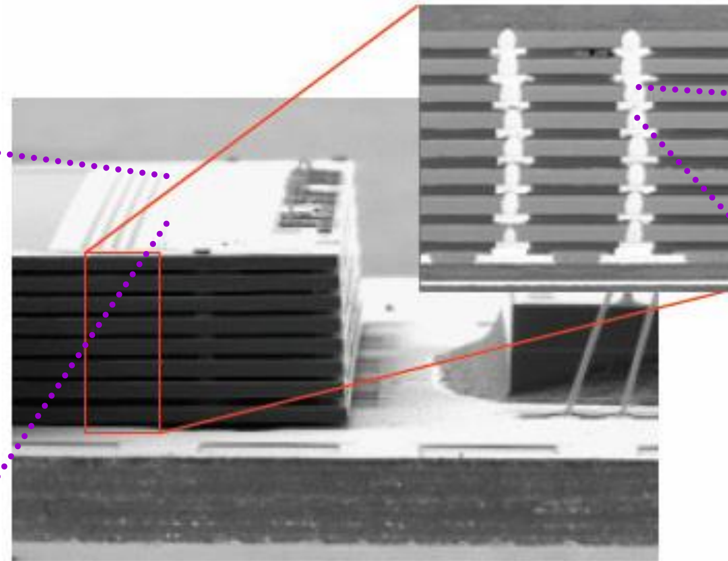
Impact on Reliability and Performance of Device

Si stress

Keep-away zone

Device must be kept away from the zone in which mobility is changed.

Si cracking

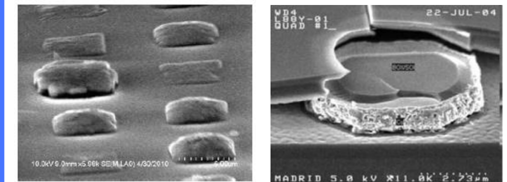


<Samsung Electronics>

Cu stress

Debonding, TSV cracking

TSV Pop-up, Bulging-up → Integration Issues

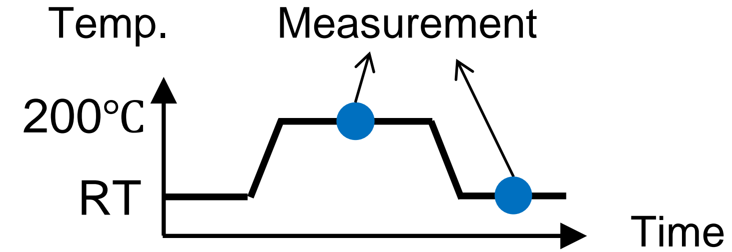


<Source: SEMATECH>

- Thermal stress of TSV → Si stress and Cu stress.
- Si stress (residual stress) → degradation of device performance.
- Cu stress (thermal stress) → mechanical failure of Cu TSV.

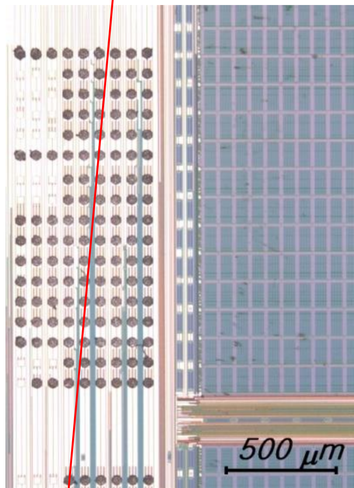
Experimental – *SK Hynix*

- Sample
  20 µm TSV diameter, 90 µm pitch, 90 µm height

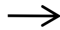


- Condition of measurement
  - Measurement of stress for : Si, Cu TSV
  - Thermal treatment : *in situ* at 200 ℃,
    ex situ for post-annealed sample (200 ℃ for 1 hour)

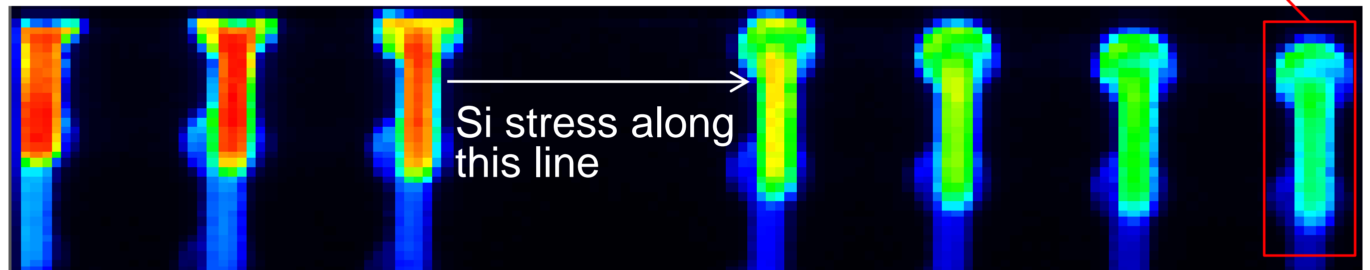
Polished with angle



Top view of TSV array



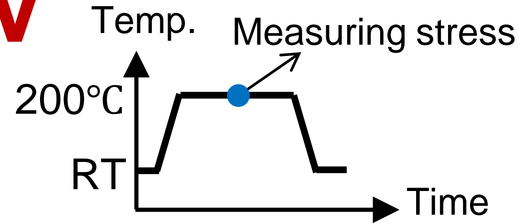
Cu stress within this area

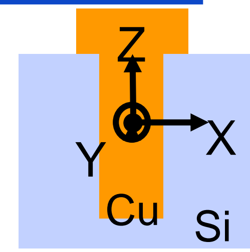


µXRD (from characteristic x-rays) image of TSV array

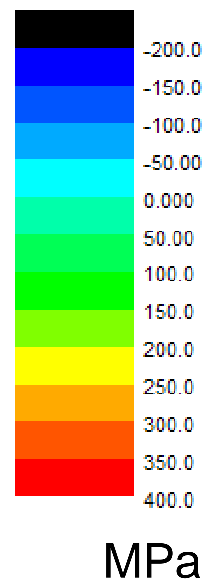
Cu Stress State in TSV

- *In situ* heating at 200 ºC





σ_{XX} σ_{YY} σ_{ZZ} σ_{XY} σ_{XZ} σ_{YZ}

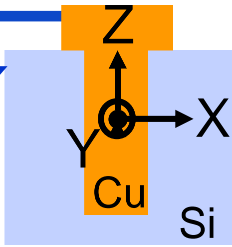


Avg. Normal Stress = 5 MPa

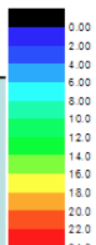
Avg. Shear Stress = 115.2 MPa

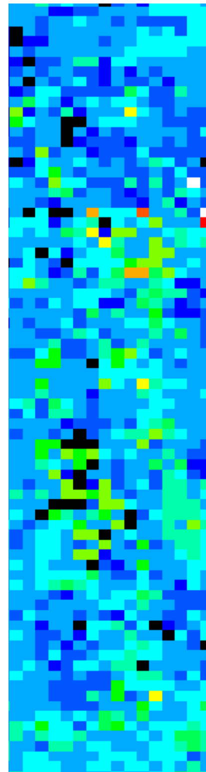
Hydrostatic stress = -195.5 MPa

Cu Stress State in TSV – *SK Hynix*
- Post Annealed Sample (measure at RT)

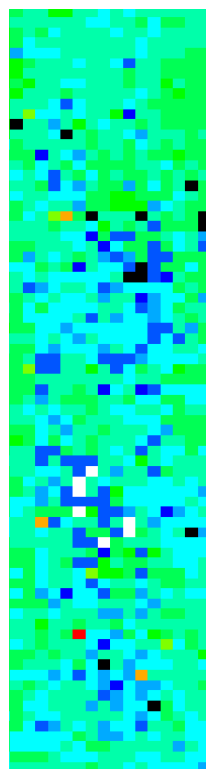


(111) in-plane orientation

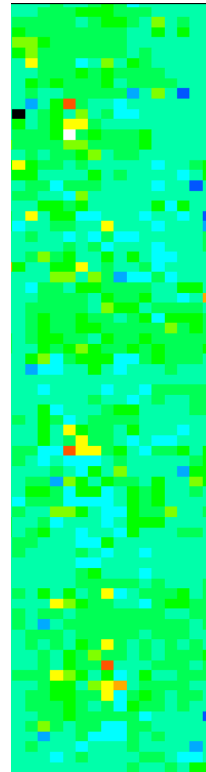




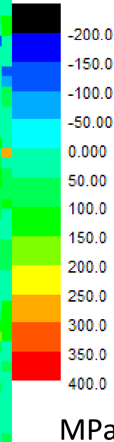
σ'_{XX}

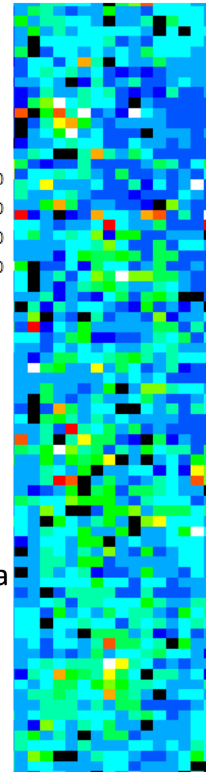


σ'_{YY}

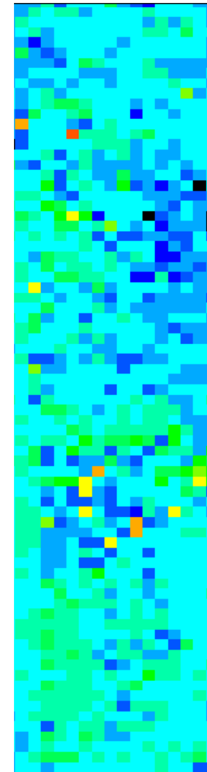


σ'_{ZZ}

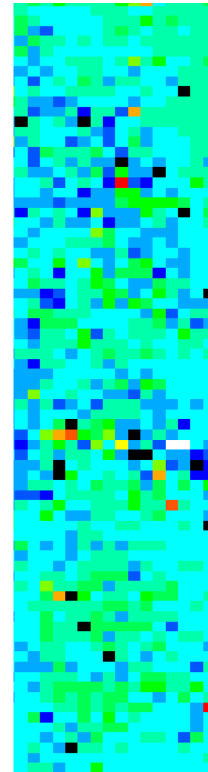




σ_{XY}



σ_{XZ}

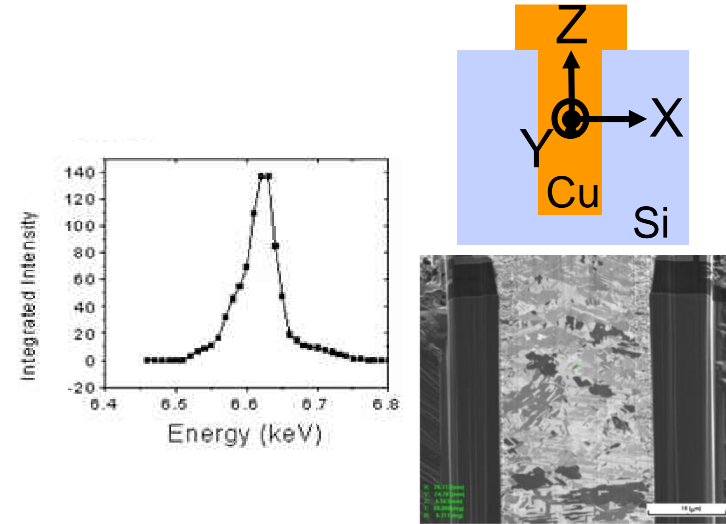


σ_{YZ}

Only deviatoric components of stress

$$\varepsilon_{ij} = \begin{pmatrix} \delta & 0 & 0 \\ 0 & \delta & 0 \\ 0 & 0 & \delta \end{pmatrix} + \begin{pmatrix} \varepsilon'_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{21} & \varepsilon'_{22} & \varepsilon_{23} \\ \varepsilon_{31} & \varepsilon_{32} & \varepsilon'_{33} \end{pmatrix}$$

Cu Hydrostatic Stress State in TSV – *SK Hynix*
- Post Annealed Sample (measure at RT)

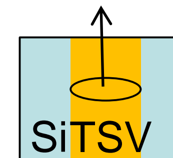


$$\varepsilon_{ij} = \begin{pmatrix} \delta & 0 & 0 \\ 0 & \delta & 0 \\ 0 & 0 & \delta \end{pmatrix} + \begin{pmatrix} \varepsilon'_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{21} & \varepsilon'_{22} & \varepsilon_{23} \\ \varepsilon_{31} & \varepsilon_{32} & \varepsilon'_{33} \end{pmatrix}$$

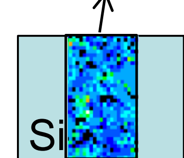
Hydrostatic stress = +166.6 MPa

- Hydro + deviatoric

One area



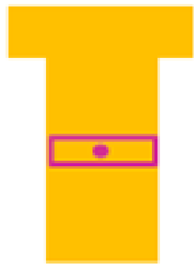
All area scan



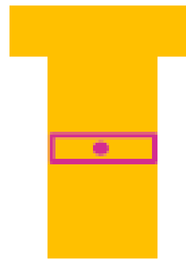
Stress Evolution in Cu TSV – *SK Hynix*

Cu hydrostatic stress

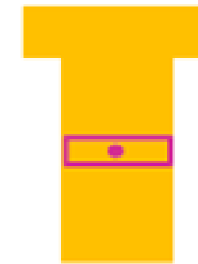
- As-received
- at 200℃
- After anealing



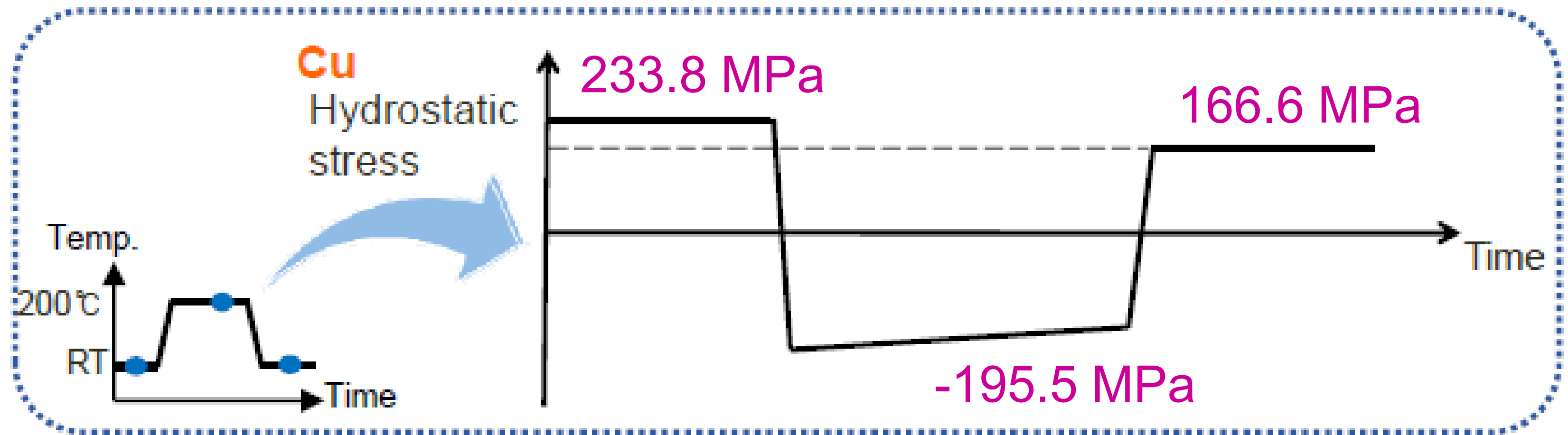
233.8 MPa



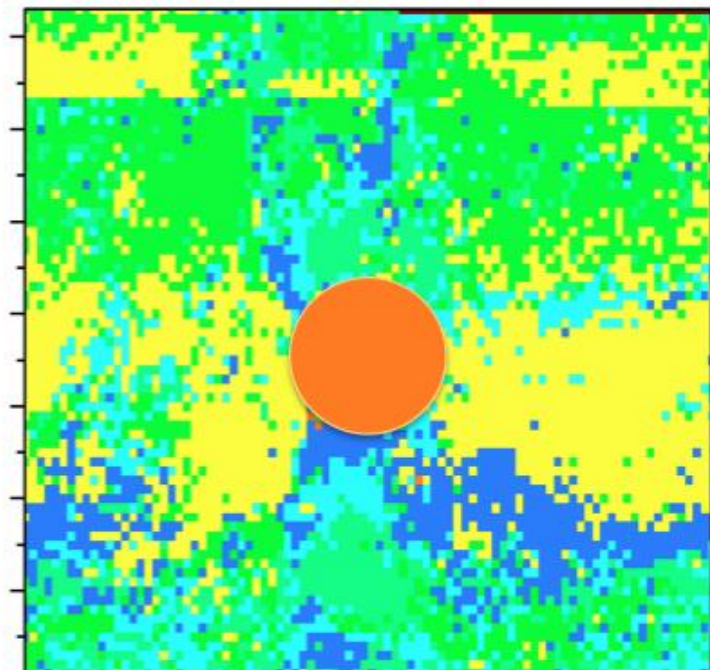
-195.5 MPa

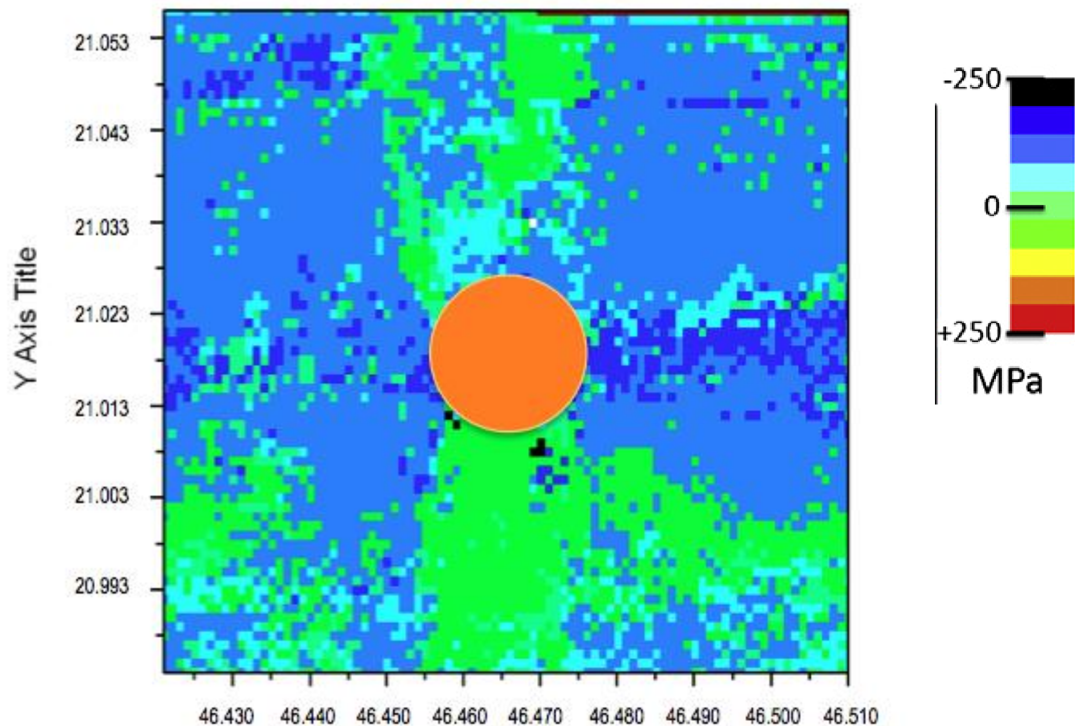


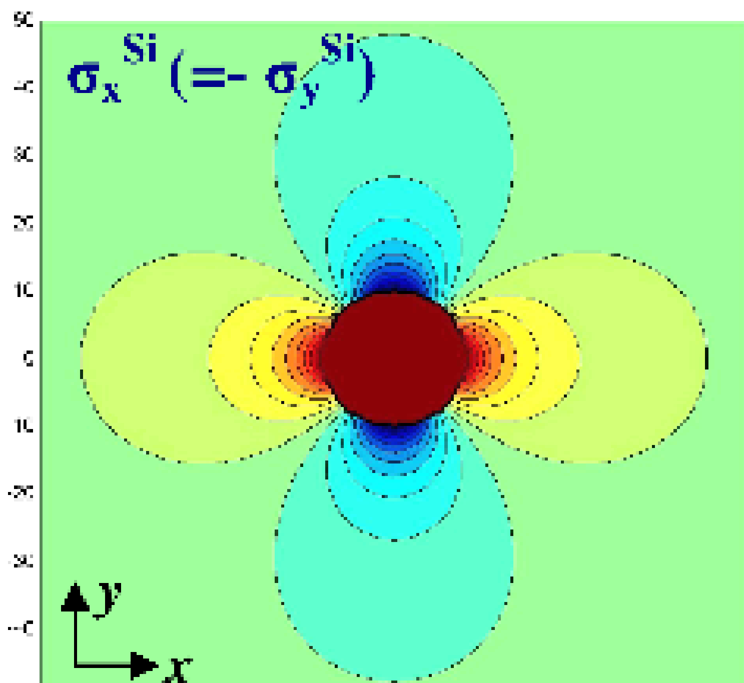
166.6 MPa

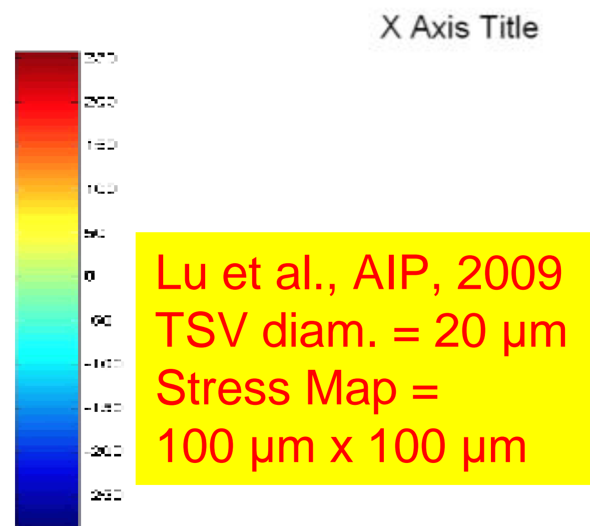


σ_{xx} (Measurement) σ_{yy} (Measurement)

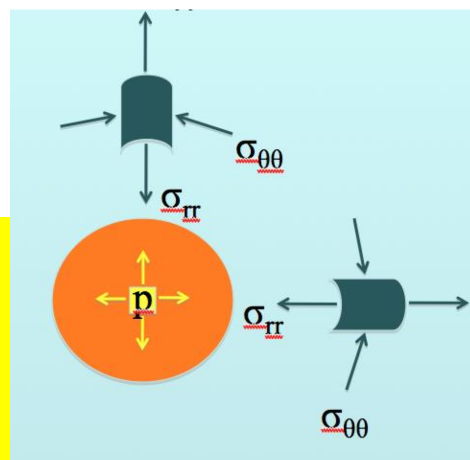






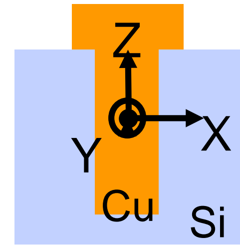


Lu et al., AIP, 2009
TSV diam. = 20 μm
Stress Map =
100 μm x 100 μm



Si Strain Profile from Edge of TSV

- Post Annealed Sample (measure at RT)



Si Strain (x 10^{-3})

0.6
0.4
0.2
0.0
-0.2
-0.4

Cu TSV

ε_{XX}

ε_{YY}

0
50
100

Distance from Edge of TSV (μm)

Si Stress (MPa)

100
50
0

Cu TSV

$\sigma_{von\ Mises}$

50
100
150

Distance from Edge of TSV (μm)

$\sigma_{\theta\theta}$

σ_{rr}

p

σ_{rr}

$\sigma_{\theta\theta}$

Si Keep-Away Zone of about **17 μm** from Edge of TSV

Summary

- Synchrotron X-ray submicron diffraction (white + monochromatic beam) has proven to be a powerful tool to measure stress states in TSV *in situ* and while the Cu via is still ***buried inside the Silicon***

- Cu stress state is mostly tensile at the post-annealed state:
  - Comparison SK Hynix vs. SEMATECH samples → RT grain growth leads to high tensile stress in the as-received state
  - How to reduce stress-induced reliability/integration → reduce Cu hydro stress in the as-received state

- Stress in Si surrounding Cu TSV was found to follow Cu hydrostatic stress: higher Cu hydrostatic stress → higher Si stress → larger "keep-away zone"
  - Si stress in array of TSV's → important for design/layout
  - Stress scanning from the top would be valuable → to optimize layout!

Acknowledgements

Sincere Thanks to - for Funding, Collaborations and Experimental Support

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SINGAPORE

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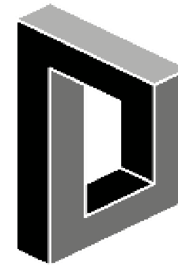
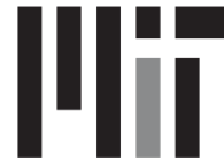
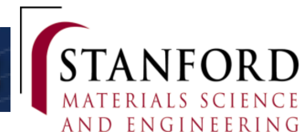


SUTD-MIT INTERNATIONAL DESIGN CENTRE (IDC)



Massachusetts Institute of Technology



Q & A

Andrew Tay

Email: andrew_tay@ieee.org

Transient Thermal Analysis

MicroSanJ

4ms @ 25% Duty Cycle

Device Excitation

1ms

t_0

CCD exposure

33ms @ 30Hz

delay

t_0

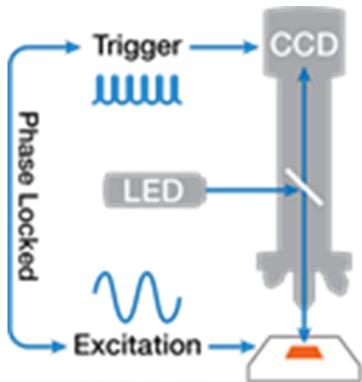
100μs

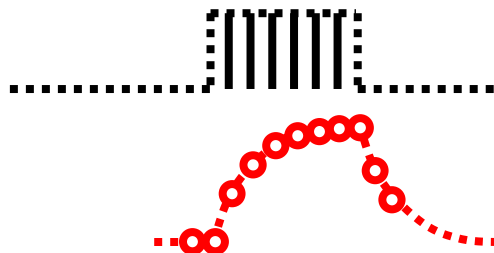
t_1

t_1

LED pulse

Temperature





- Acquisition timing (shift cycle by cycle)
- Device temperature data points