Recent Advances in GaN Power HEMTs Related to Thermal Problems and Low-Cost Approaches

WW05

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Thermal management of electronics: Measurement and the limits of GaN-on-diamond electronics

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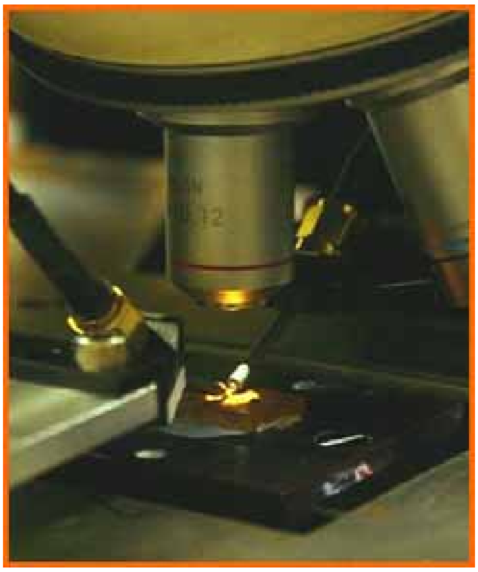
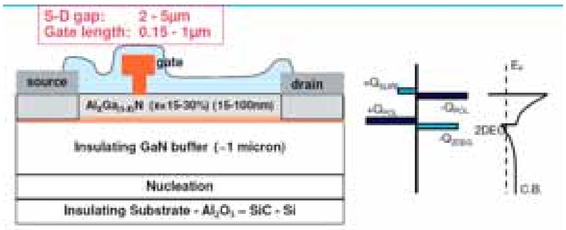
Outline

- GaN electronics
- Thermal management challenges
- Thermal materials and device characterization
- Ultra-high power electronics: GaN-on-Diamond HEMTs
- Conclusions



Microwave GaN Electronics



You can buy this already (GaN-on-SiC, GaN-on-Si) !!!

Thermal management

Electronic Warfare

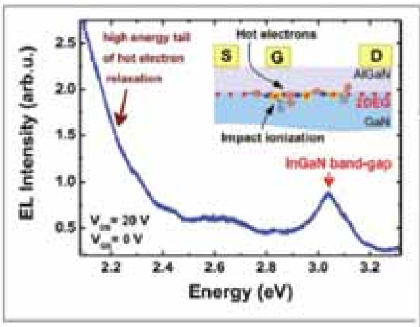
Directed Energy Systems

Radar Systems

Challenges: New material and device design; **how to measure channel temperature of a device ?**

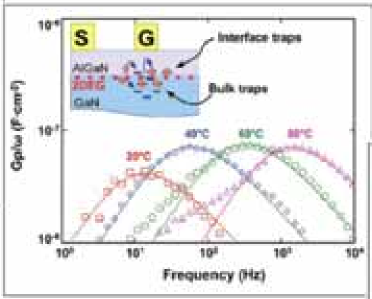
Performance and reliability

Impact ionization

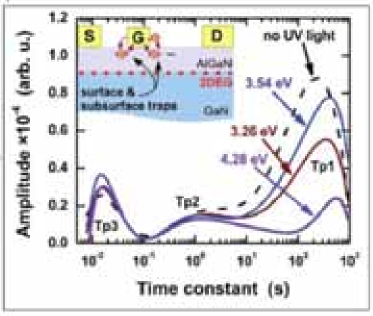


Killat et al., Compound Semiconductor
Jan/Feb 2013

Bulk trap generation

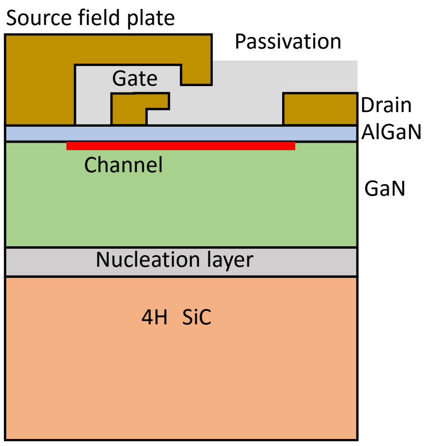


Interface trap generation



Device degradation is temperature and electric field accelerated.

Electric field & temperature

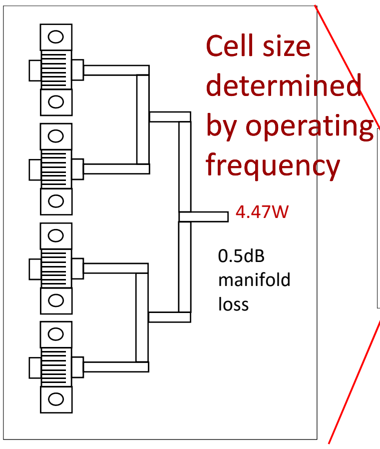


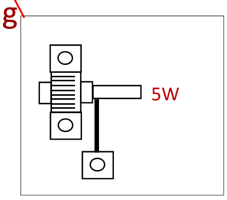
Electric fields can be 'shaped' using e.g. field plates, T-shaped gate, slanted gate i.e., electric field driven device degradation can be limited.

Temperature is the main factor
at present limiting the reliability ie determining the maximum possible power density.

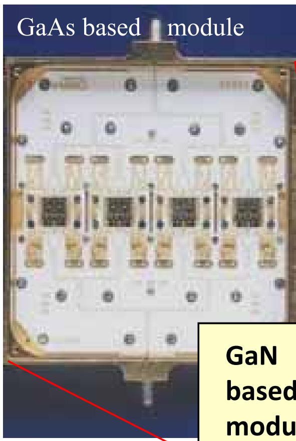
GaN HEMT thermal history

Worked example 20W 10GHz solid-state module





GaN HEMT
Vds=28V (5W/mm)
1 x 1mm transistor
Zopt=50ohm // 0.2pF



GaN based module

PRESENTLY
4x reduction
in size

GaAs pHEMT
Vds=8V (0.9W/mm)
4 x 1.38mm transistor
Zopt=4.5ohm // 1.1pF

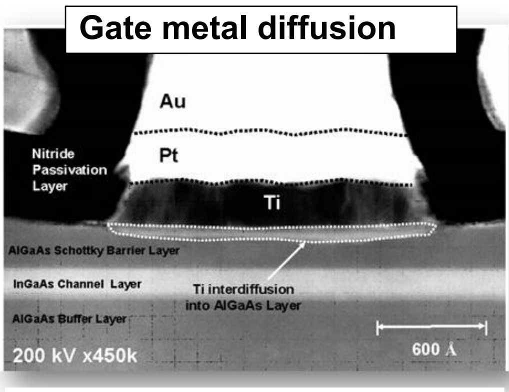
GaAs (0.5 W/mK) thermal conductivity much lower than GaN-on-SiC (1.6; 4.5 W/mK).

Is this the limit

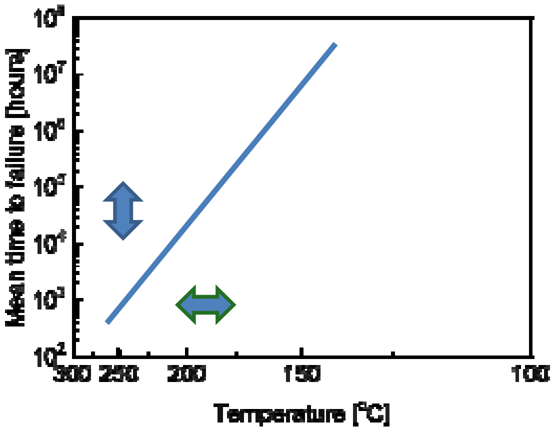
Channel temperature

Device degradation determined buy temperature

Rate of device failure $\propto$ exp($-E_a/k_BT$), **with E_a = activation energy**
T = channel temperature (or temperature at specific location inside channel).

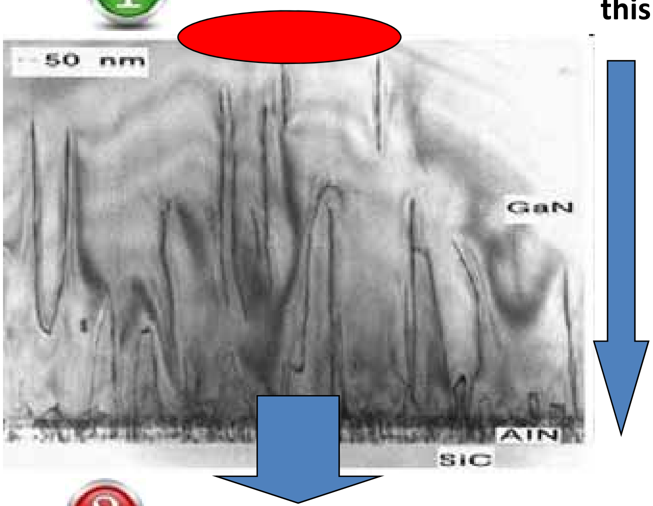


J. A. del Alamo et al., IEEE IEDM 2004



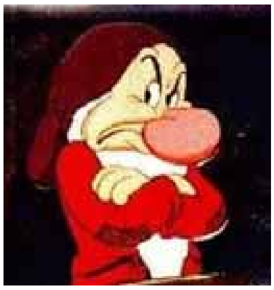
Why waste with experiment

1 Heater width ?



3 Heat has to traverse interfaces

2 I can do a thermal simulation …
this saves me a lot of money and time



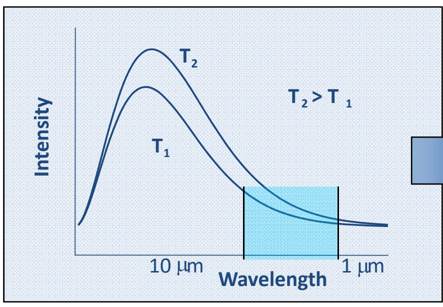
Thermal conductivity of material and variation through layer(s)

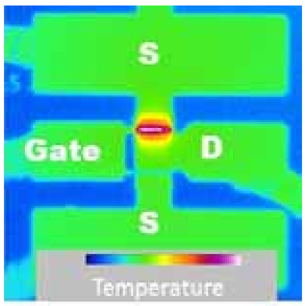
IR Thermography

Basic principle: Measures intensity of thermal IR radiation

$$u(\nu, T) = \frac{8\pi h\nu^3}{c^3} \frac{1}{\exp\left[\frac{h\nu}{k_B T}\right] - 1}$$

Measured intensity $j = \sigma T^4$
with σ Stefan-Boltzmann constant



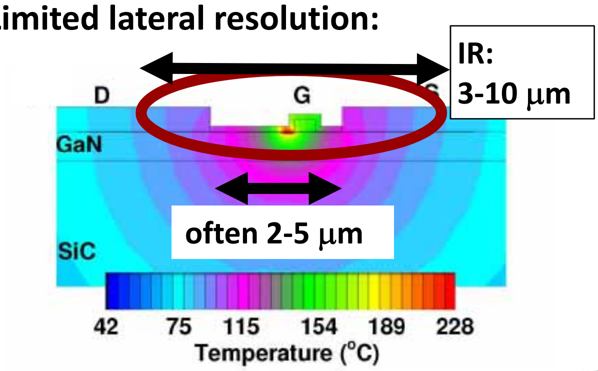


Often 3-5 µm or 8-10 µm spectral window is used.

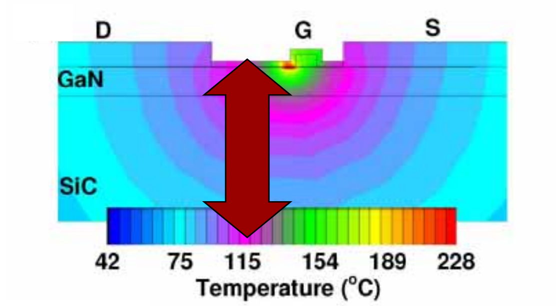
Fast, but **diffraction-limited spatial resolution of >3-10 µm.**

IR Thermography

Limited lateral resolution:



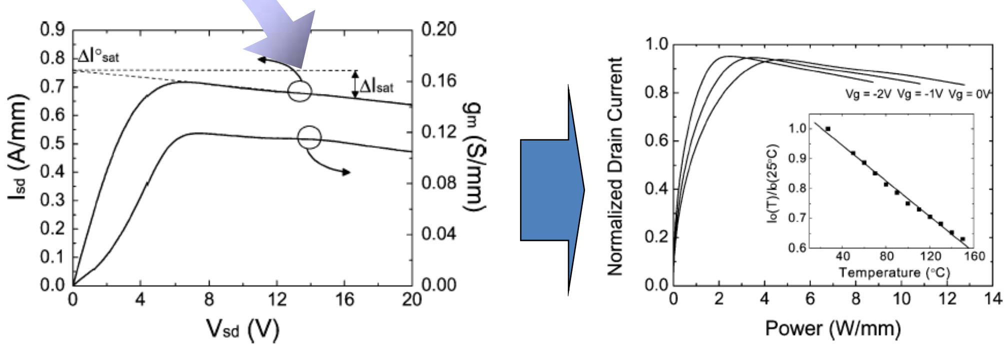
Typical 'no' depth resolution (for uncoated devices):



IR measures a temperature average which is often not easy to define.

Electrical Methods

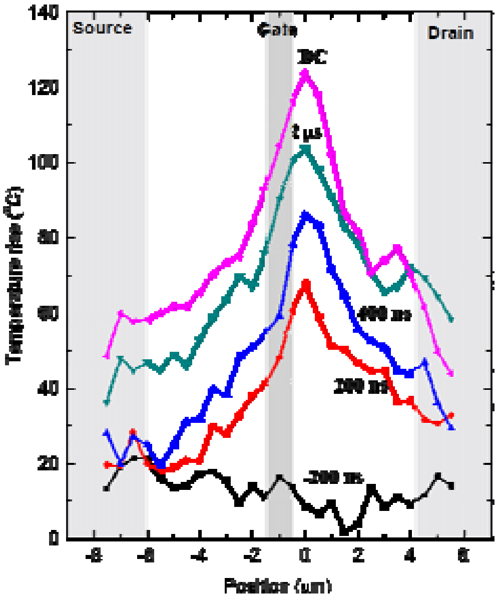
Basic principle: Quantifies **changes in IV curve with temperature rise**, e.g., a change in saturation current.



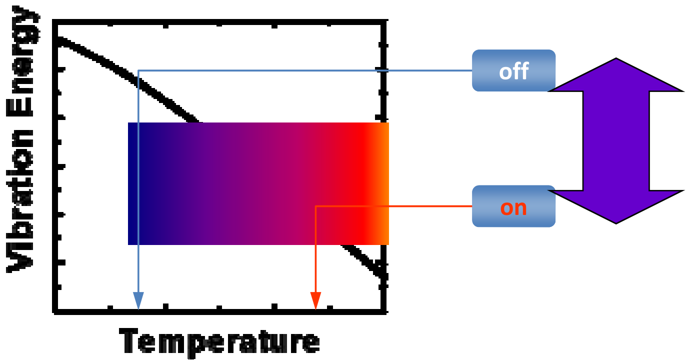
E.g. Kuzmik et al, IEEE Trans. Electron Dev.48 1496 (2002); McAllister et al., J. Vac. Sci. Techn. 24, 624 (2006); Simms, IEEE Trans. Electron Dev. **55**, 478 (2008).

Advantage: Uses **electrical test equipment standard in most laboratories**; measures however **average temperature over whole device**.

Raman thermography



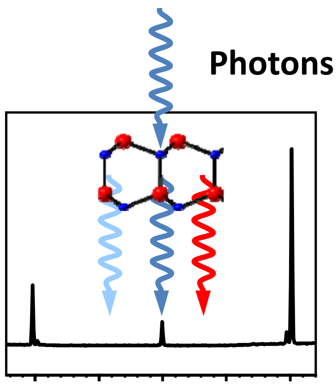
Based on that vibrations of 'atoms' (phonons) of materials are temperature dependent



- Spatial resolution ~ 0.5-0.7 µm.
- Temperature resolution < 2-5 °C.
- Time resolution ~ 10 ns.
- Easy to use.

The Raman method

Photons of a laser 'hit' device



Photon energy change

Scattered light contains three different wavelengths

Light of same photon energy as laser

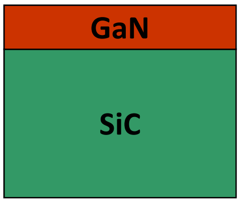
Light of reduced photon energy (photon created a vibration of 'atoms')

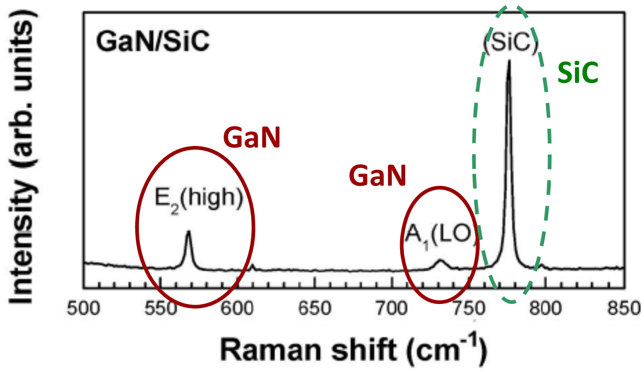
Raman probes typically this light

Light of increased photon energy (photon absorbs a vibration of 'atoms')

M. Kuball, Surf. Interface Anal. **31**, 987 (2001).

A typical Raman spectrum



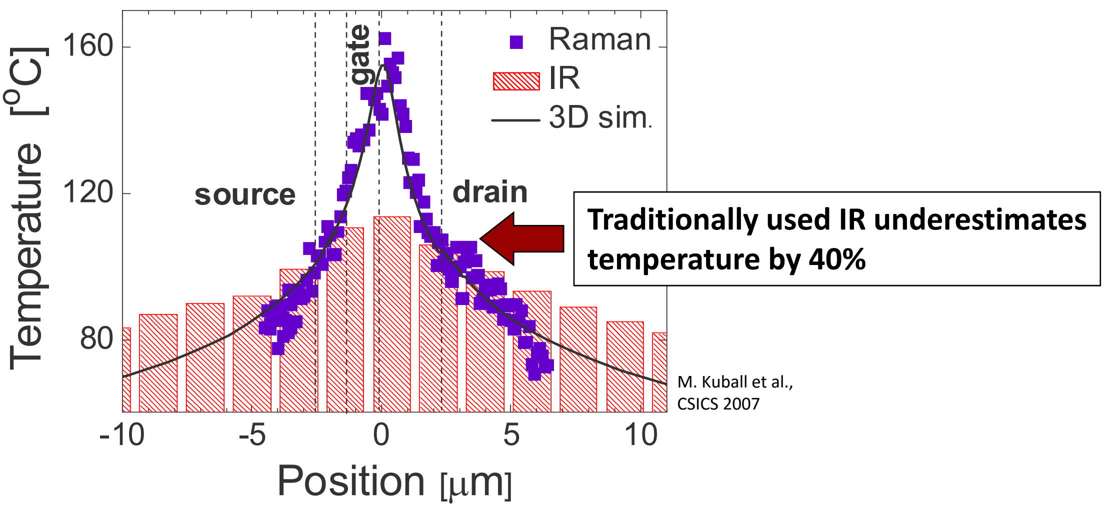


Temperature in ‘all’ different material layers in a device can be probed simultaneously:

- **GaN, SiC temperature in GaN/SiC HEMT**,
- **AlGaAs, GaAs temperature in GaAs pHEMT**,
- **…**

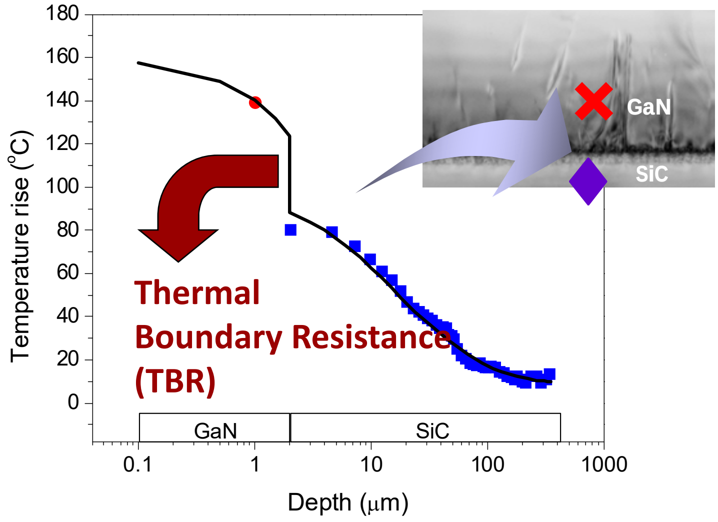
Raman vs IR thermography

AlGaN/GaN HEMT on SiC

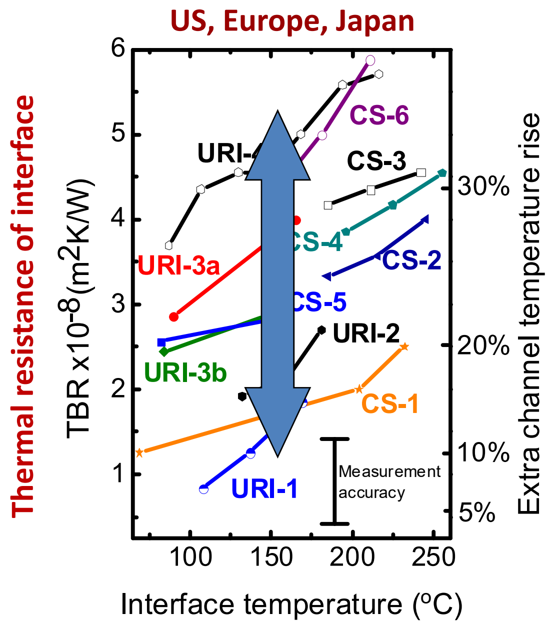


Spatial resolution: Raman ≈0.5-0.7 µm IR ≈7 µm.

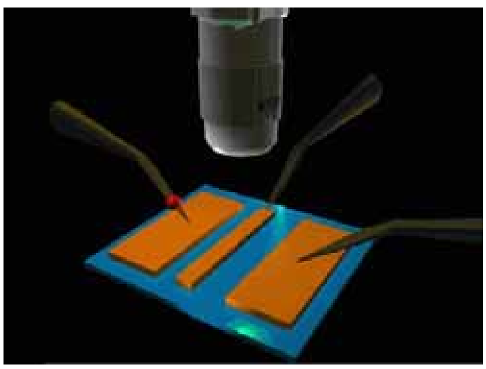
Importance of interfaces



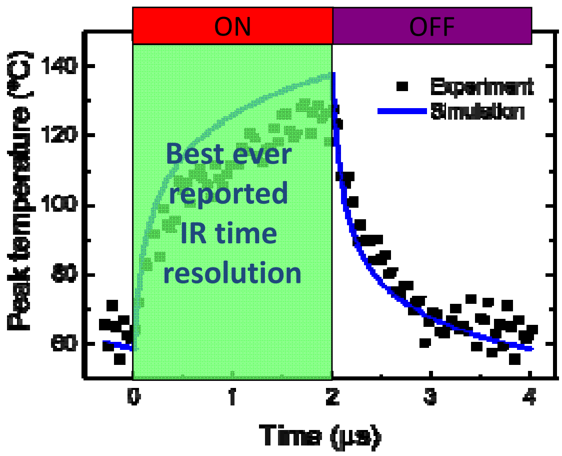
Manoi et al., IEEE Electron Dev. Lett ***31****, 1395 (2010).*



How to obtain time resolution



Time resolution: 10 ns.
Spatial resolution: 0.5 µm.

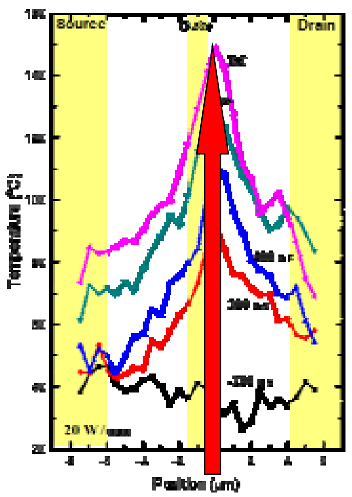


Order of magnitude faster and more accurate than other thermography techniques.

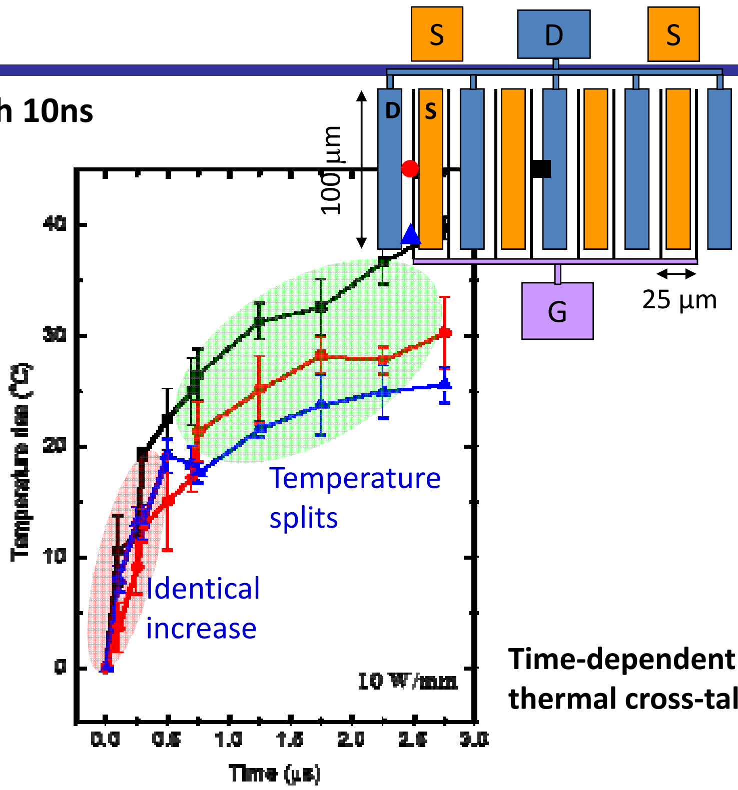
Riedel et al., IEEE Electron Dev. Lett. **29**, 416 (2008); Kuball et al. IEEE Electron Dev. Lett. **28**, 86 – 89 (2007).

Time-resolved Raman

Ability to trace temperature with 10ns time resolution

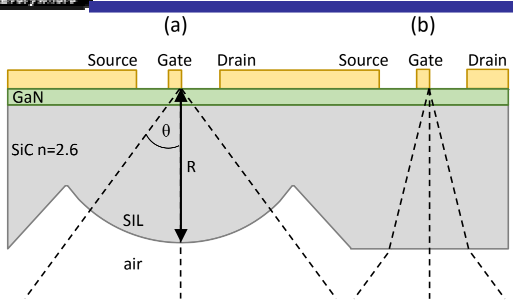


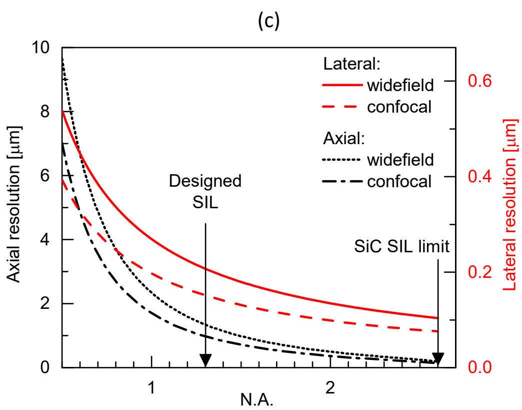
Manoi et al, Solid State Elecronics **57**, 14 (2011).



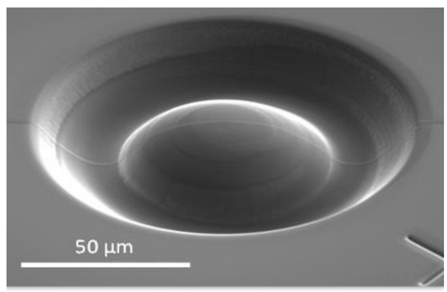
Time-dependent thermal cross-talk

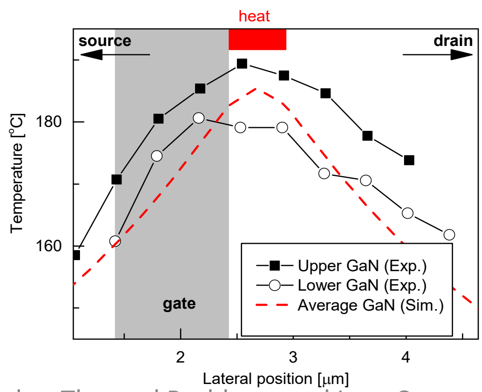
Can one improve resolution ?





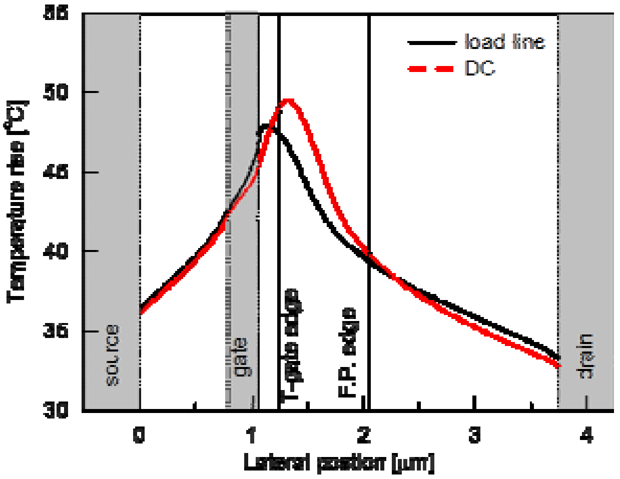
Solid Immersion Lens (SIL)

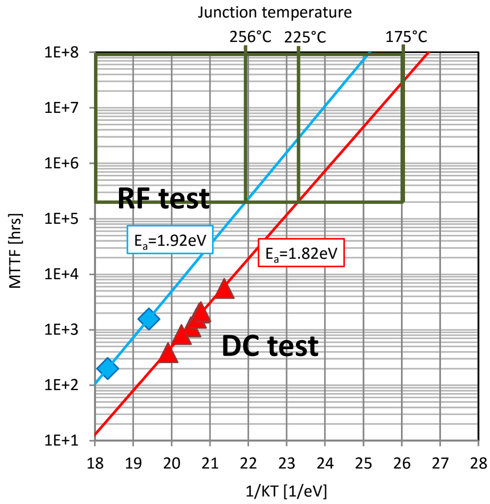




J.W. Pomeroy et al., J. Appl. Phys. **118**, 144501 (2015)

DC vs RF temperatures

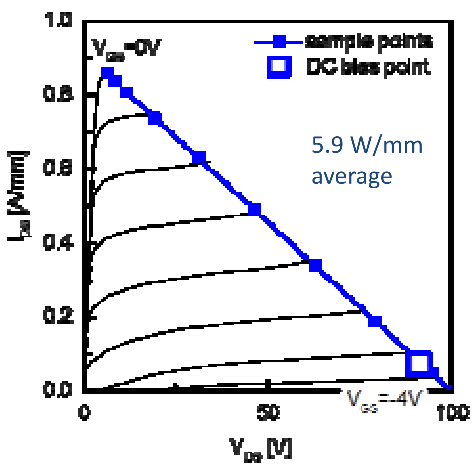




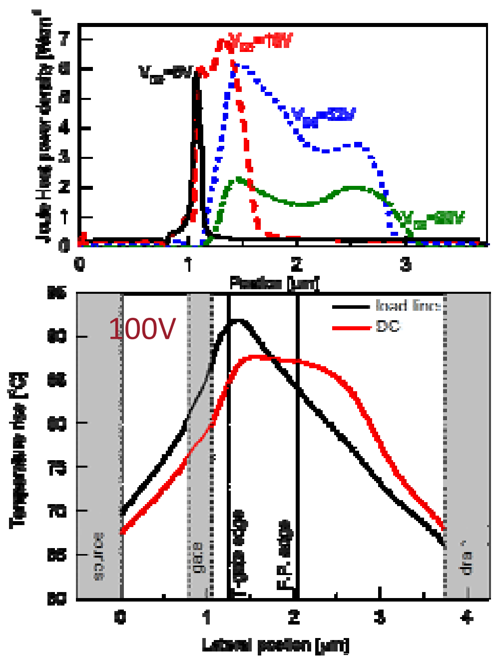
Activation energy determined in DC and RF lifetime test similar.

J.W. Pomeroy, Microelectronics Reliability **55**, 2505 (2015).

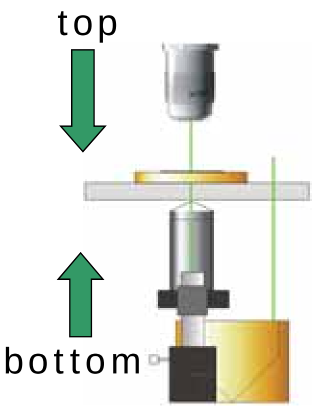
However, for >100V

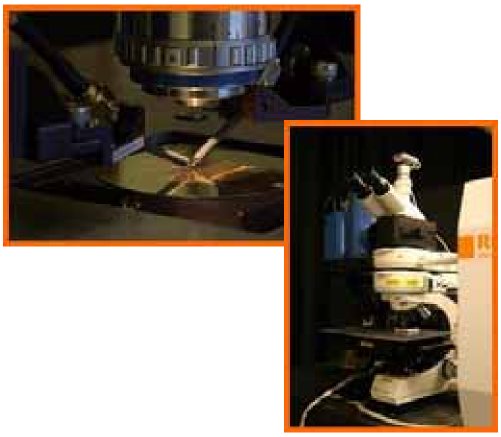


J.W. Pomeroy et al. ROCS 2015.



How to do it in real life ?

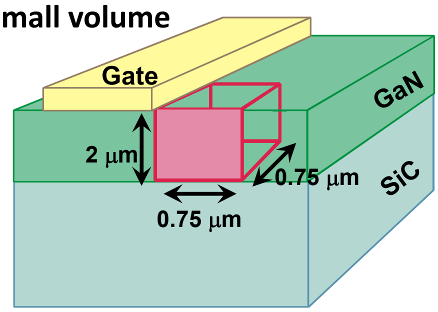




Can be performed on-wafer or in-package. Only condition is that the semiconductor of the device is optically visible.

Temperature measured

For optically transparant materials – Average of temperature in small volume

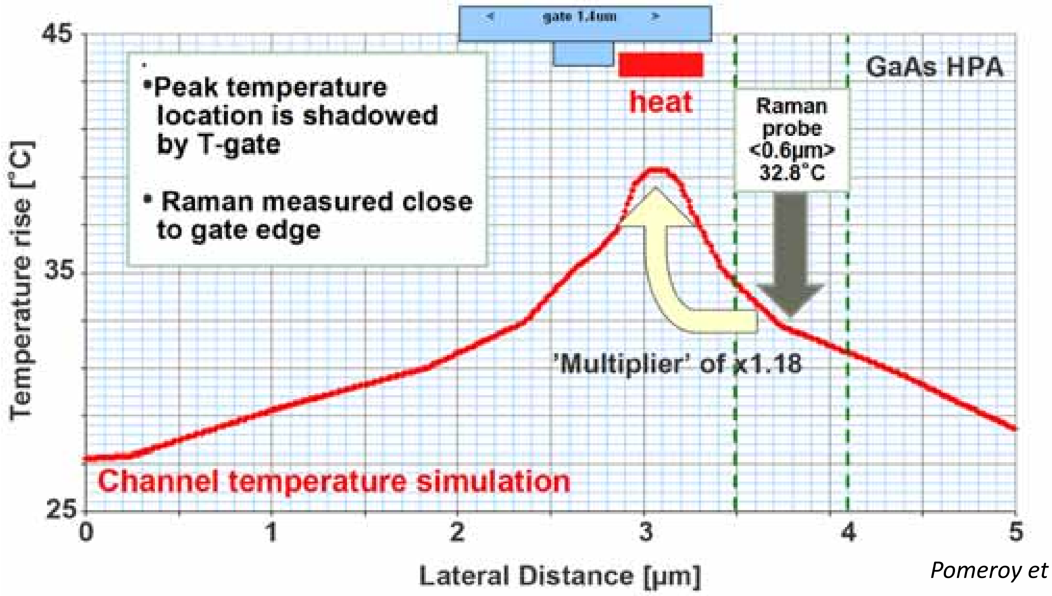


For optically non- transparant materials – Small 'surface' area

Temperature average over 0.75 μm x 0.75 μm x 50nm (for GaAs)

It is well defined over which area an average of temperature is measured and should be compared a subsequent thermal simulation !!!

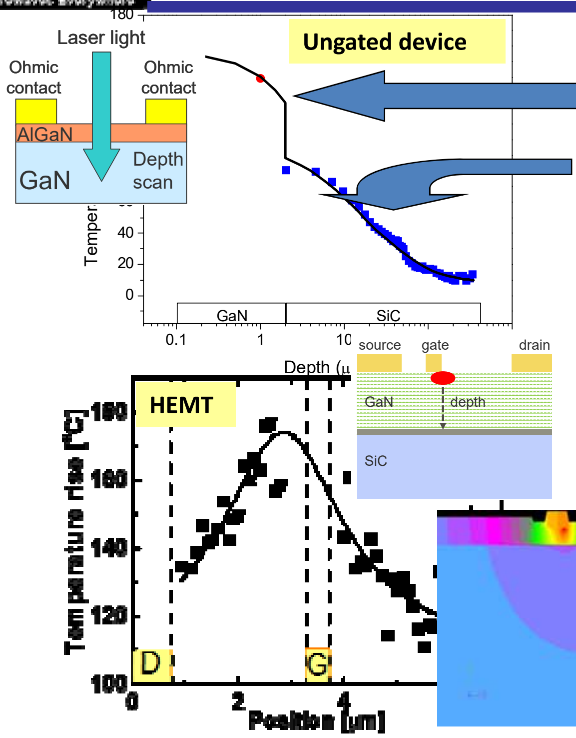
Simulation to aid experiment



Pomeroy et al, IMS 2012

If there is a T-gate or field plate, we consider this by using thermal simulation, as those 'screen' the hot spot.

Methodology developed …

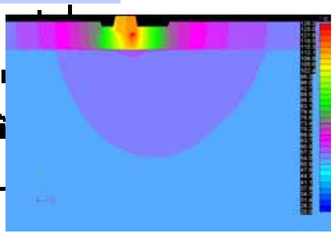


Step 2 – We fit in thermal simulation **any resistances at internal chip interfaces.**

Step 1 – We fit in thermal simulation the gradient in temperature through SiC to extract **SiC thermal conductivity.**

Extract key material parameters

Step 3 – We measure **temperature in active device region** and determine **Edge of Chip (EoC) temperature** (temperature 500 µm away from device).

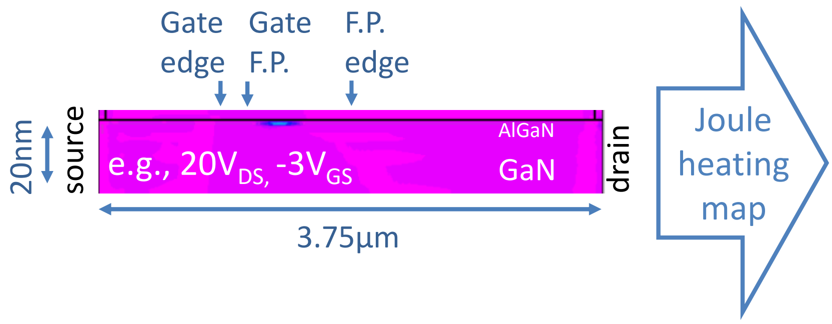


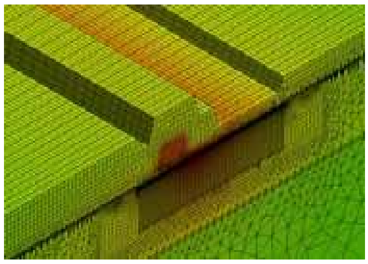
Step 4 – We **fit thermal simulation to HEMT and EoC temperature**; EoC temperature considers die attach.

Thermal simulation

2D drift-diffusion model

3D finite element thermal model



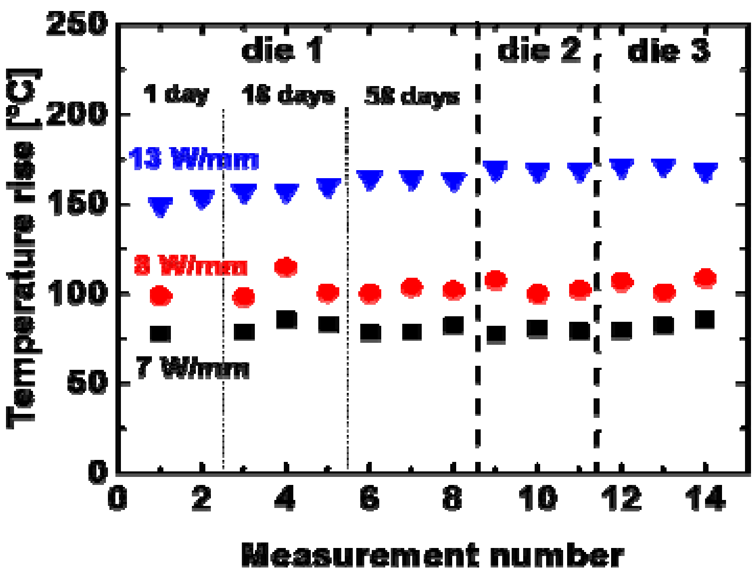


Calibrated 3D thermal model including die and package

This approach combines the advantage of accurate P_{diss} profile (drift-diffusion) with 3D finite element, e.g. large models

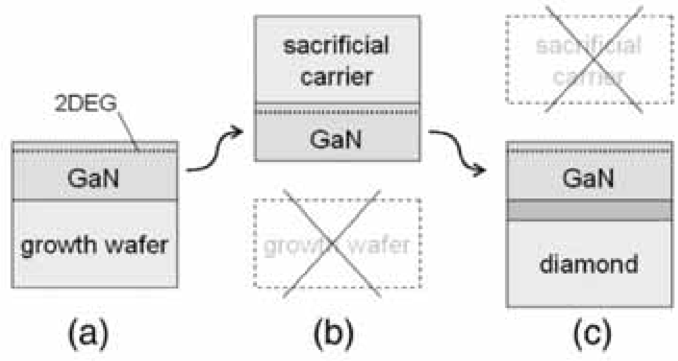
J. W. Pomeroy *et al.*, *Microelectron. Reliab.*, **(55)12**, 2505 (2015).

Good repeatability

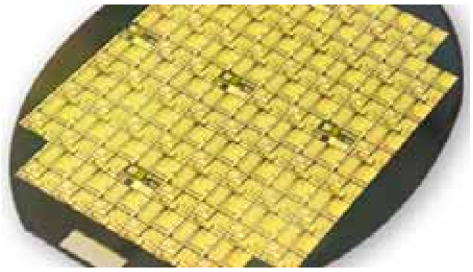


≤ ±5°C

GaN-on-Diamond HEMT



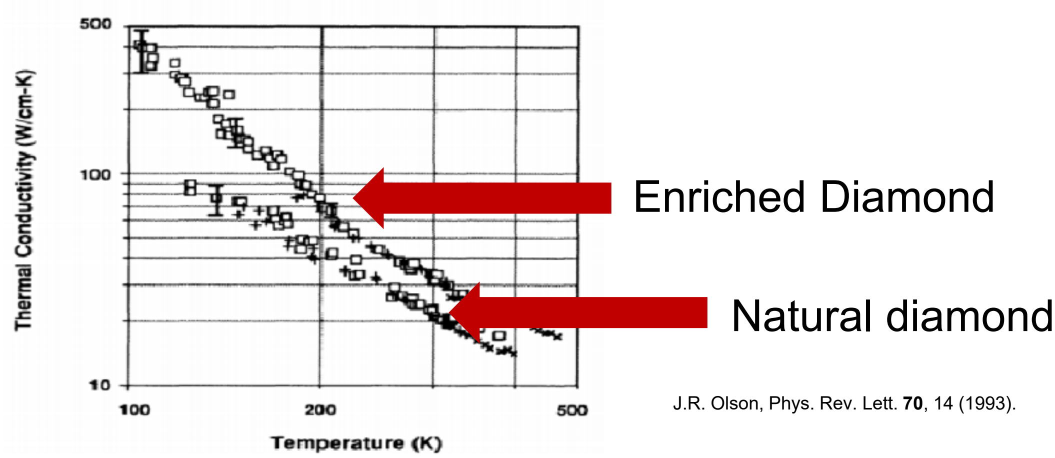
Qorvo & Bristol, CSICS 2013;
Pomeroy et al, Appl. Phys. Lett. **104**, 083513 (2014).



A 3× power density increase was achieved by the DARPA NJTT program

Thermal conductivities

Single crystalline diamond



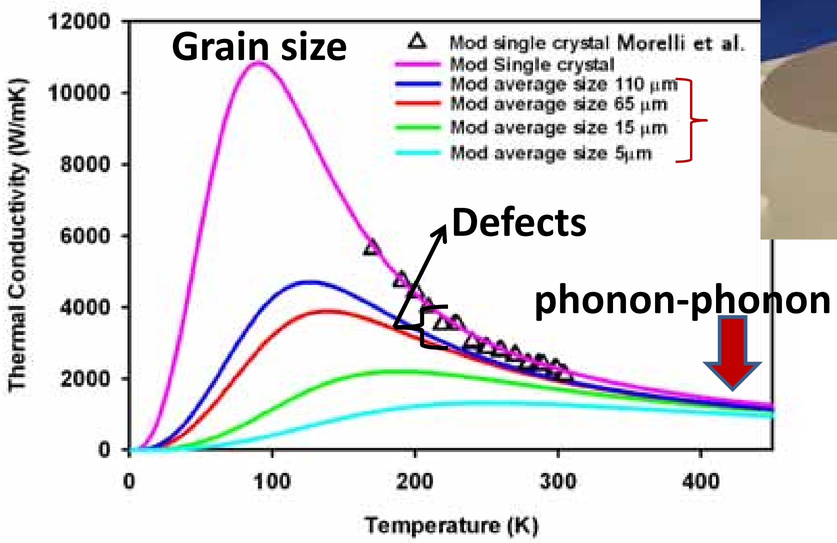
J.R. Olson, Phys. Rev. Lett. **70**, 14 (1993).

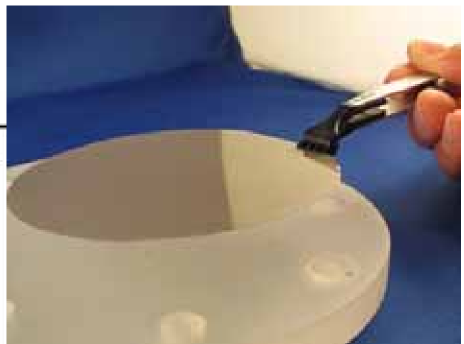
SiC thermal conductivity: 4.8 W/cmK

Single-crystalline diamond

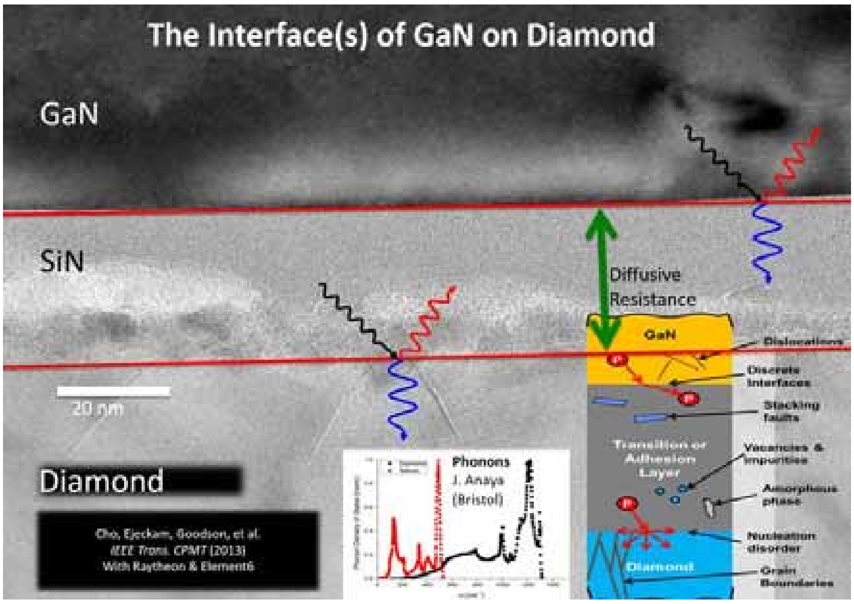
Not a realistic option to use for semiconductor technology

Poly-crystalline diamond

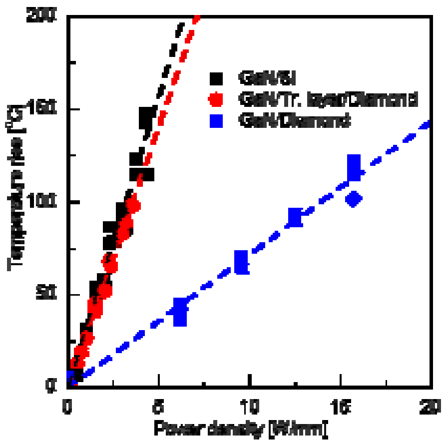


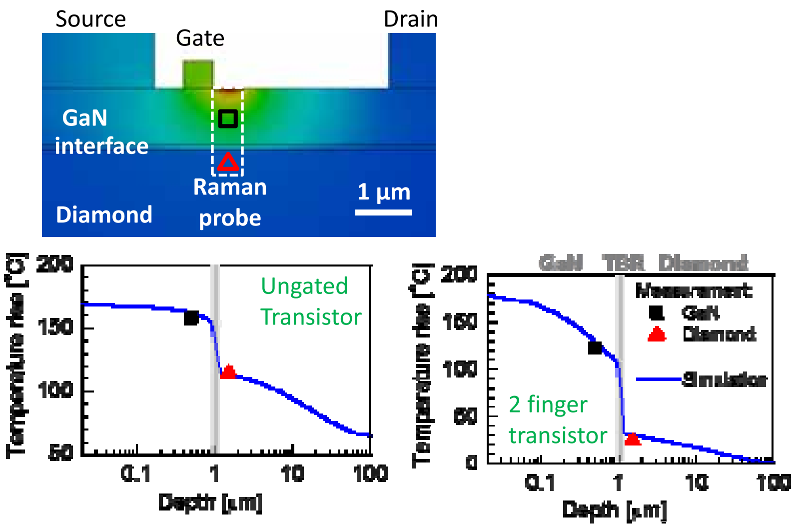


The role of interfaces



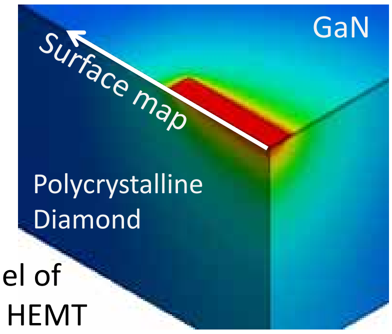
Importance of interfaces



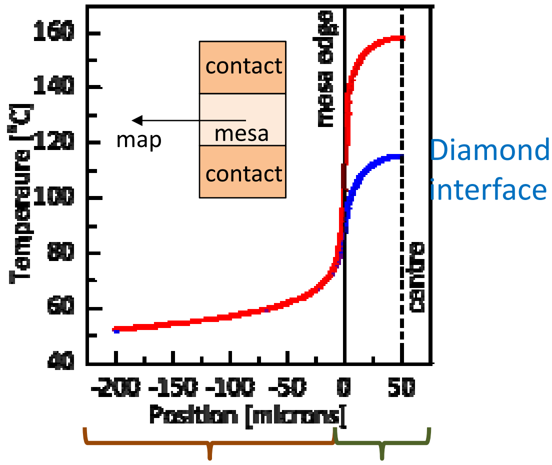


Polycrystalline diamond properties as well as interfaces need to be optimized.

Diamond thermal conductivity



F.E. model of ungated HEMT ¼ cross section



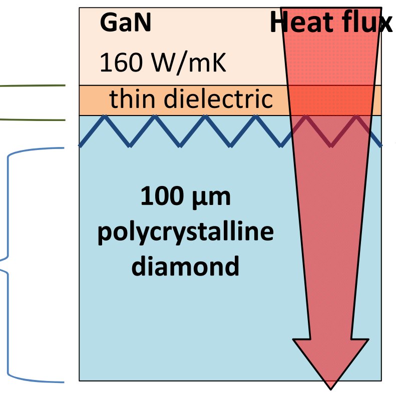
Fit finite element model by adjusting two parameters: → Diamond thermal conductivity + GaN/diamond interface TBR_{eff}

Pomeroy et al, CSICS 2014.

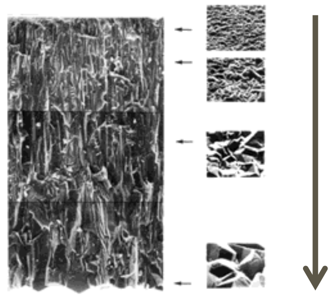
Diamond thermal properties

TBR_{eff}: Effective thermal boundary resistance

Effective thermal conductivity: Weighted average, influenced by grain size.



Increasing thermal conductivity along growth direction



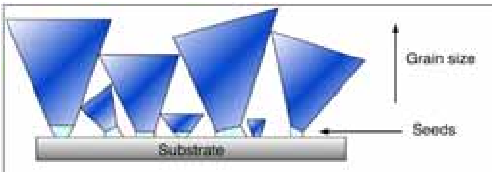
O.W. Kiiding et al.Diamond Relt.Mater., 3 (1994) 1178

	Substrate T.C. [W/mK]	TBR_{eff} $\times10^{-8}$ [m^2K/W]
GaN-on-SiC	420	2-5 (~2.5 typical)
GaN-on-di	**1200 (effective)**	**2.7±0.3**

(Pomeroy et al., CSICS 2013)

REMINDER:
Bulk diamond:
2000-3000 W/mK

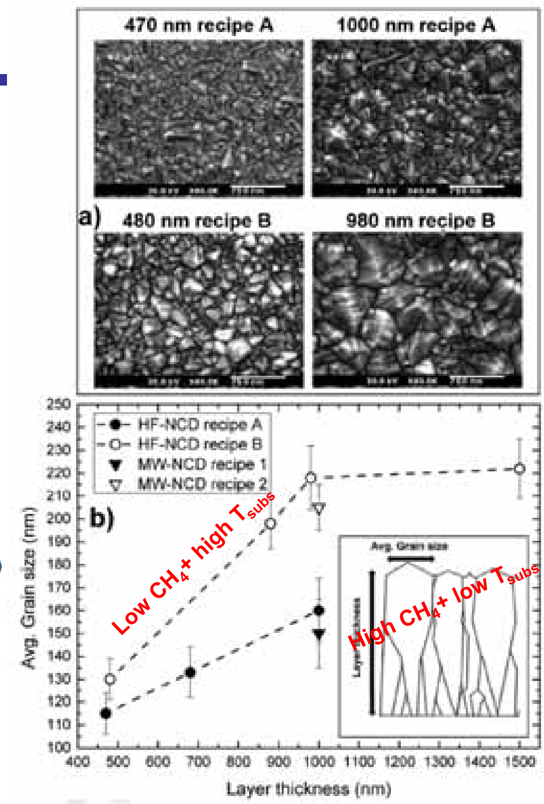
Near nucleation diamond



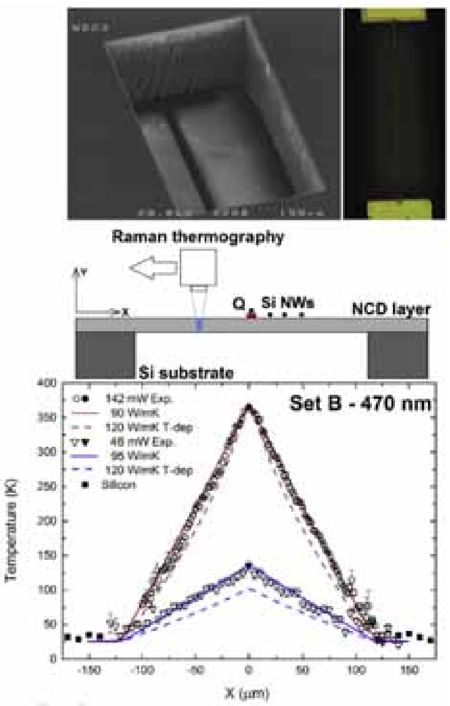
Thermal conductivity impacted by grain size

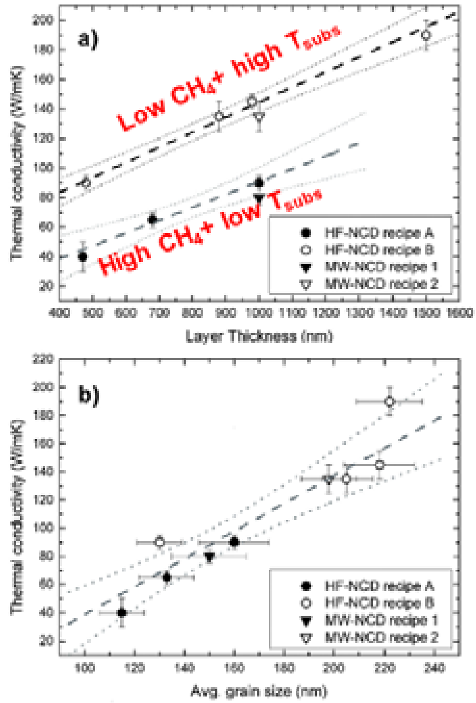
Grain evolution can be controlled by manipulating the chemistry of the diamond growth.

J.Anaya et al. Acta Materiala **103**, 141 (2016); Appl. Phys. Lett. **106**, 223101 (2015).

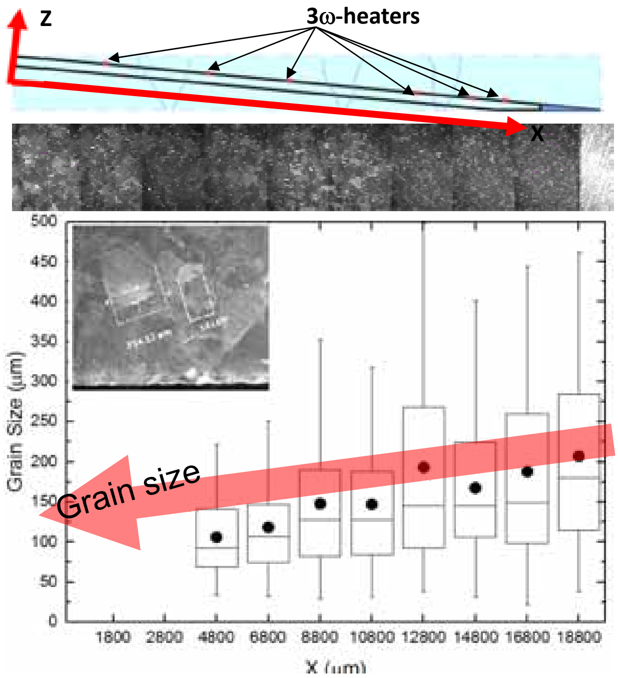


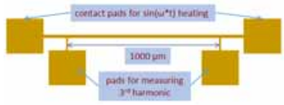
Near nucleation diamond





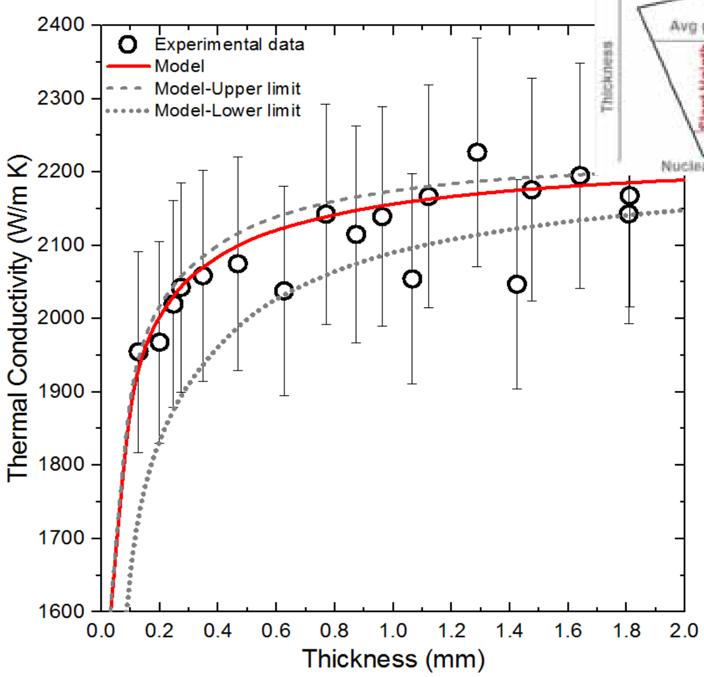
Diamond beyond nucleation

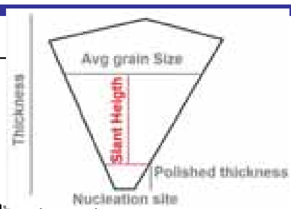


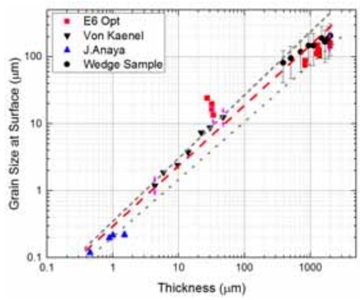


Thermal conductivity. determined by **3-omega technique**.

Diamond beyond nucleation





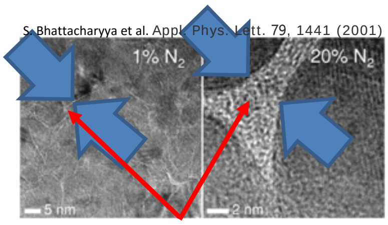


R.Baranyai et al. APEX ***9****, 061302 (2016)*

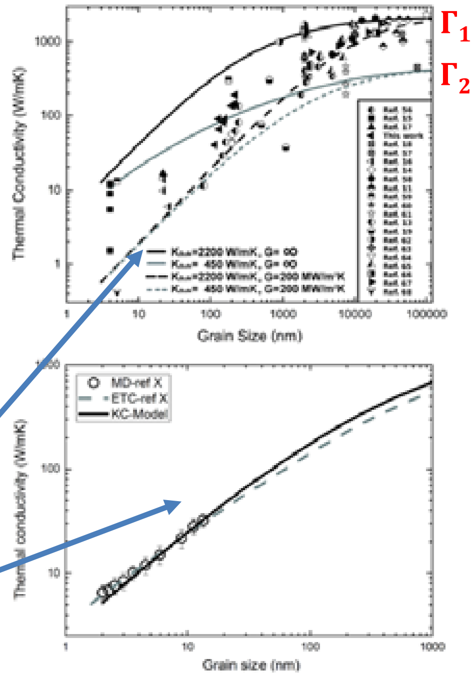
Modeling of diamond properties

(i) **thermal resistance between grains,**

(ii) **shortening in the phonon mean free path due the reduced size of the grains**



Grain Boundary thickness



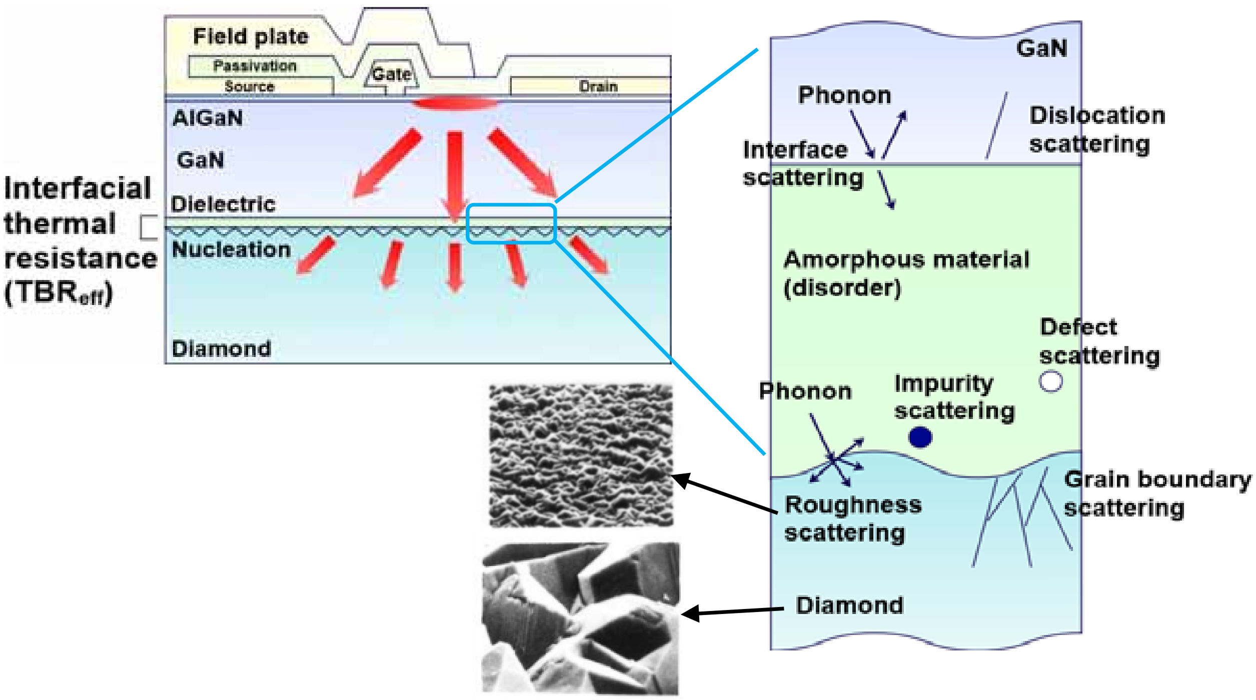
Callaway

$$k^{KC}(T,\Gamma,L_{eff},G) = \frac{k^{C}(T,\Gamma,L_{eff})}{1+\frac{k^{C}(T,\Gamma,L_{eff})}{L_{eff}\times G}}$$

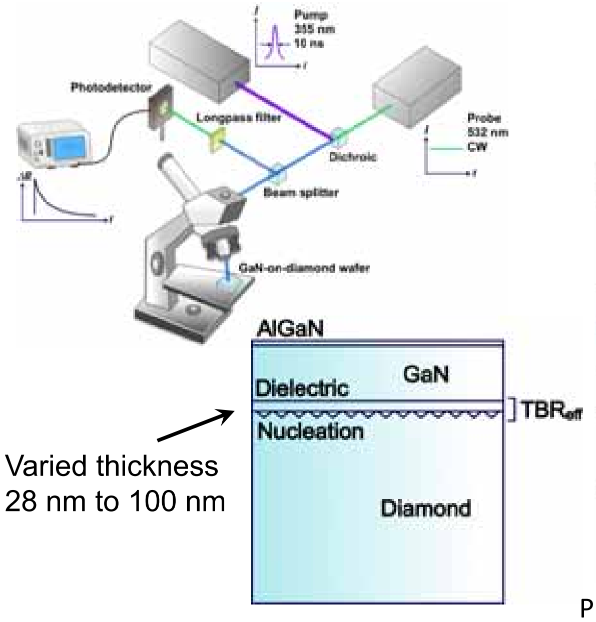
Kapitza-like

J.Anaya et al., Acta Materiala **103**, 141 (2016).

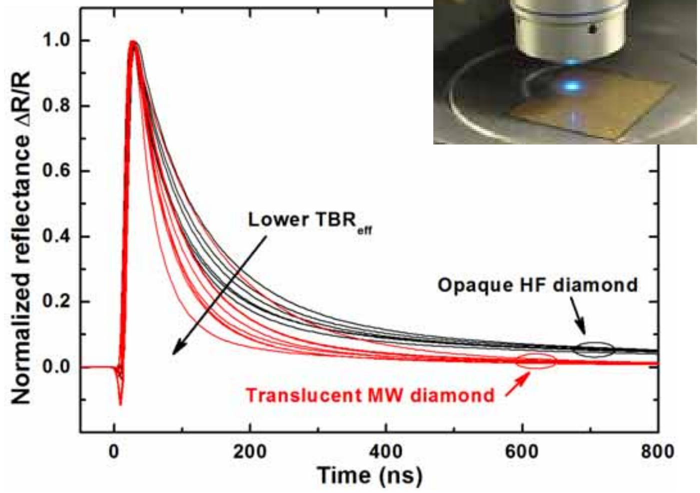
GaN-diamond interface



Transient Thermoreflectance



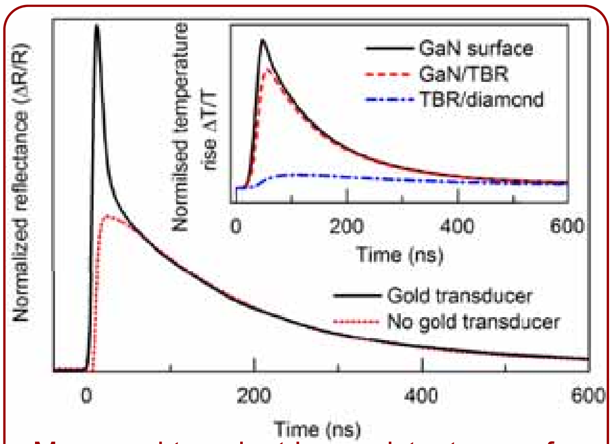
Wafer mapping & fast wafer screening



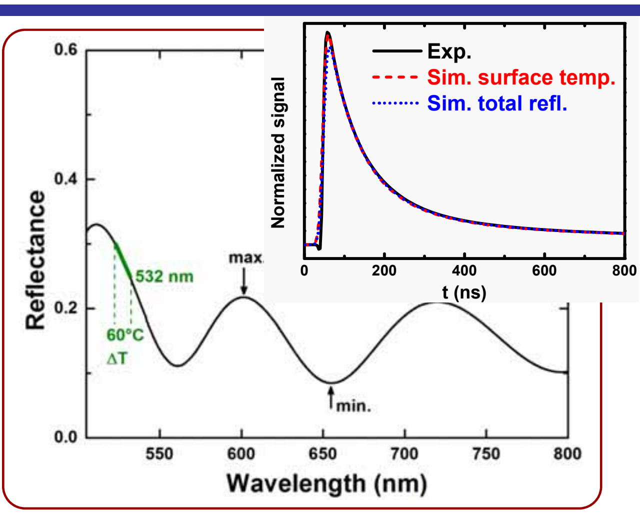
Presently we develop this into a commercial equipment.

Sun et al. IEEE Electron Dev. Lett. (accepted) 2016; Appl. Phys. Lett. **106**, 111906 (2015); Pomeroy et al. IEEE Electron Dev. Lett. **35**, 1007 (2014).

Validation of the technique



Measured transient is consistent on wafers w/ and w/o gold transducer

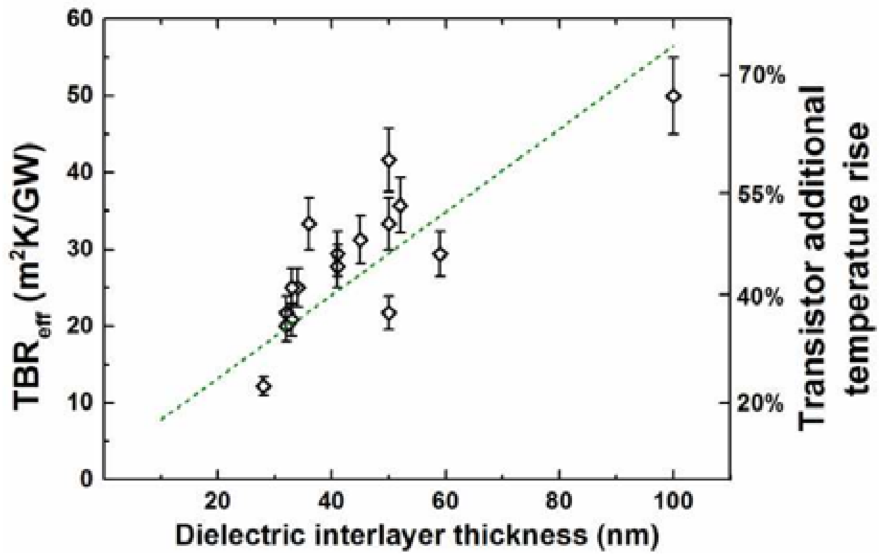


Precautions have been taken to ensure that the measured signal represents the surface temperature transient.

- **Different UV powers result in identical transients.**
- **Thermo-optic simulation further supports data.**

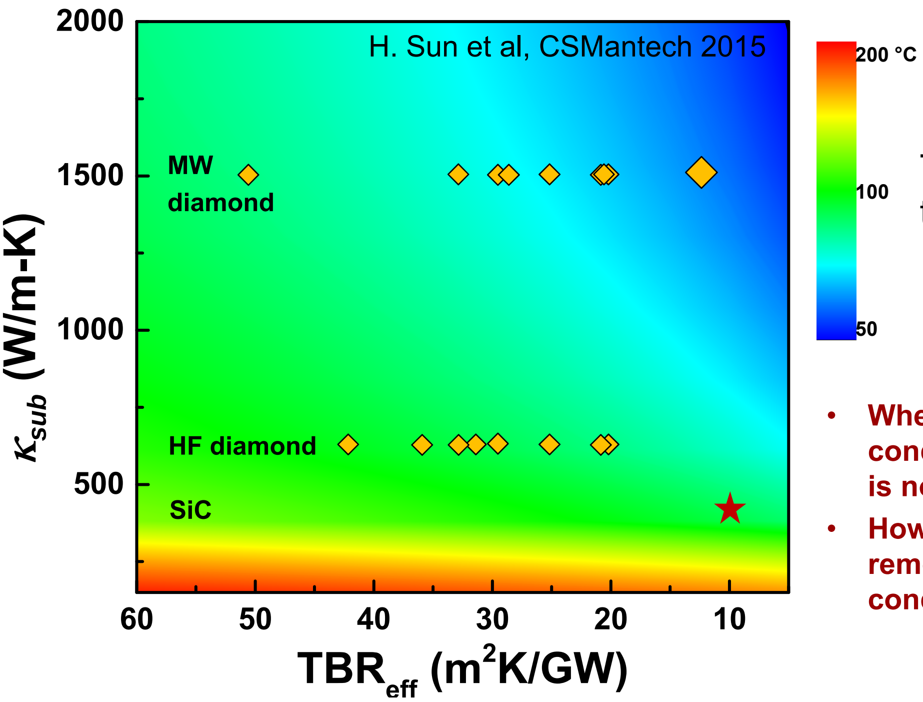
H. Sun et al, CSMantech 2015

GaN-diamond interface



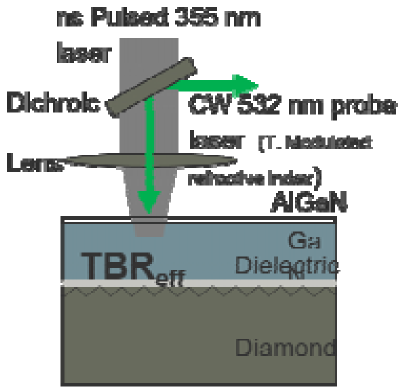
Dielectric seeding layer needs to be optimized.

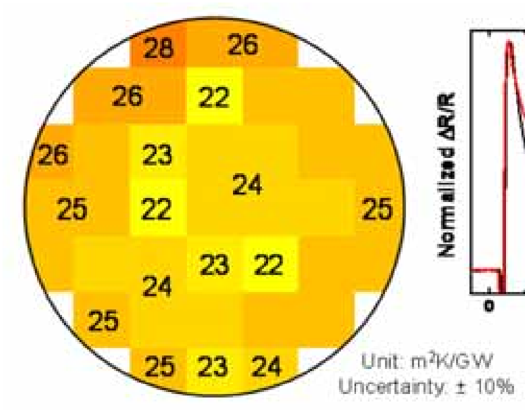
GaN-diamond interface

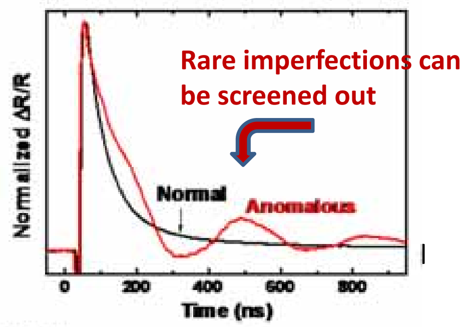


- **When substrate thermal conductivity is low, TBR$_{eff}$ is not the major factor.**
- **However, TBR$_{eff}$ limits heat removal for high thermal conductivity substrates.**

Wafer screening



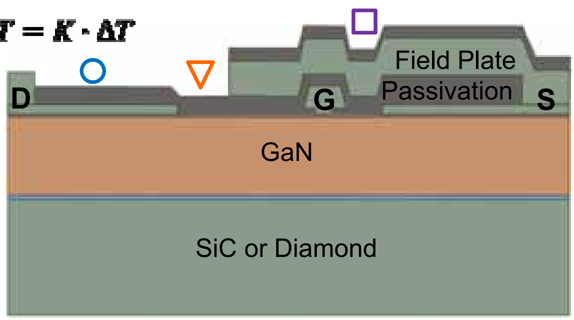




Fast wafer-mapping of the GaN-on-Diamond thermal resistance

Thermoreflectance for devices

$$\frac{\Delta R}{R} = \left(\frac{1}{R}\cdot\frac{\partial R}{\partial T}\right)\cdot \Delta T = K \cdot \Delta T$$

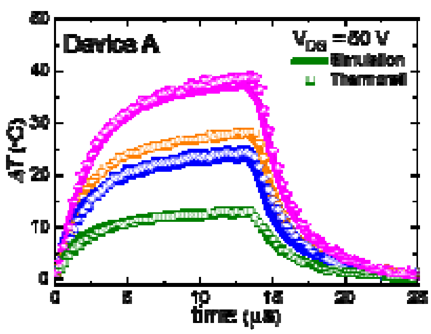


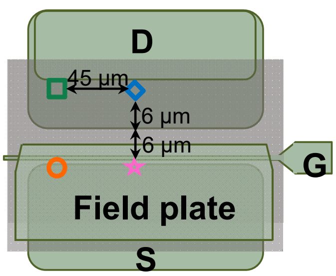
Materials:

- Two metallization levels:

1. Drain contact (○)
2. Source field plate (□)

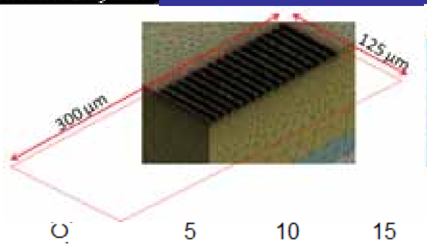
- GaN (▽)

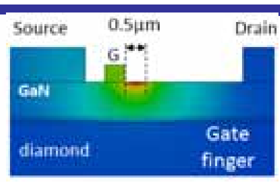


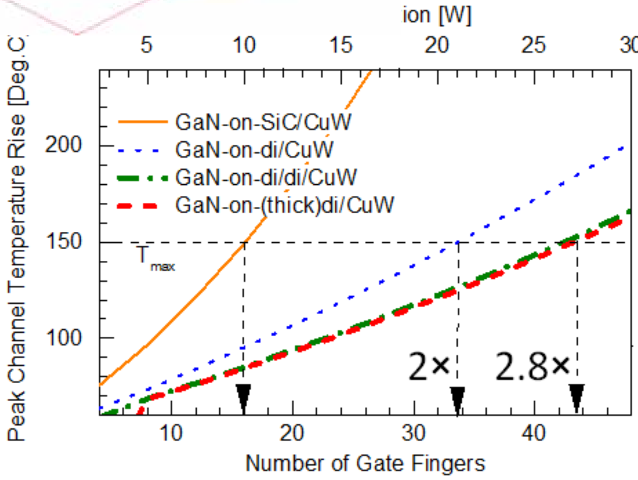


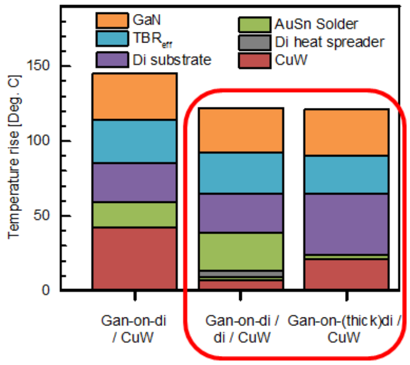
S Martin Horcajo et al., CS Mantech 2016

GaN-diamond HEMT design







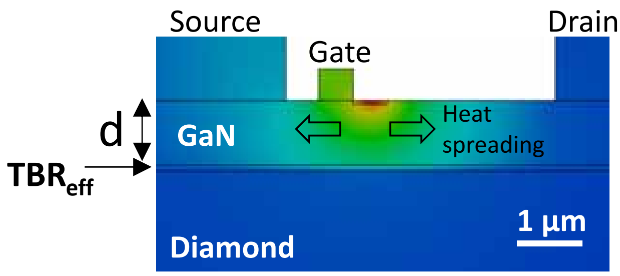


J. W. Pomeroy et al, CSICS 2014

Decreasing thermal resistance associated with the carrier enables a further

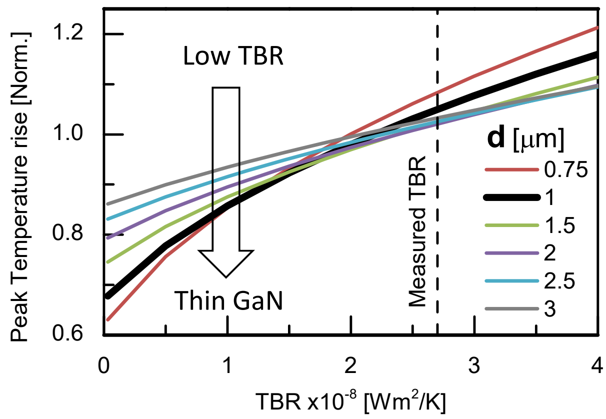
Increase in power density to ~3X

GaN layer optimization



e.g. 4 Finger HEMT

Vary GaN buffer thickness (d) and TBR_{eff}



A 1µm-thick GaN buffer is optimal for the range TBR_{eff} values expected

J. W. Pomeroy et al, CSICS 2014

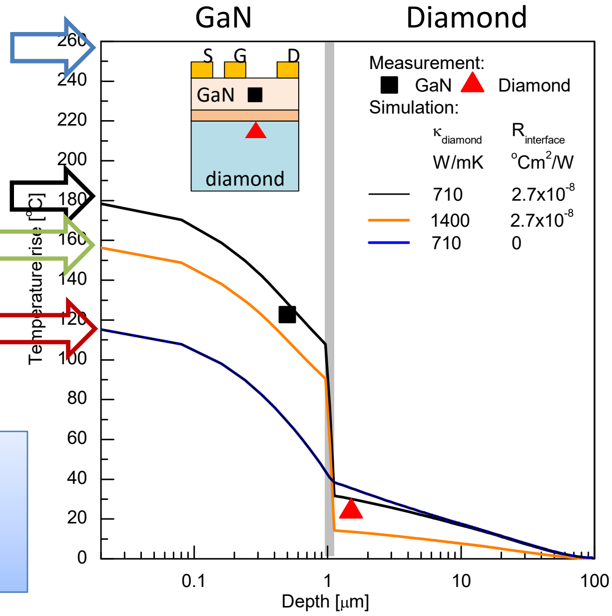
Raman experimental validation

GaN-on-SiC

Current GaN-on-diamond

Increasing diamond thermal conductivity

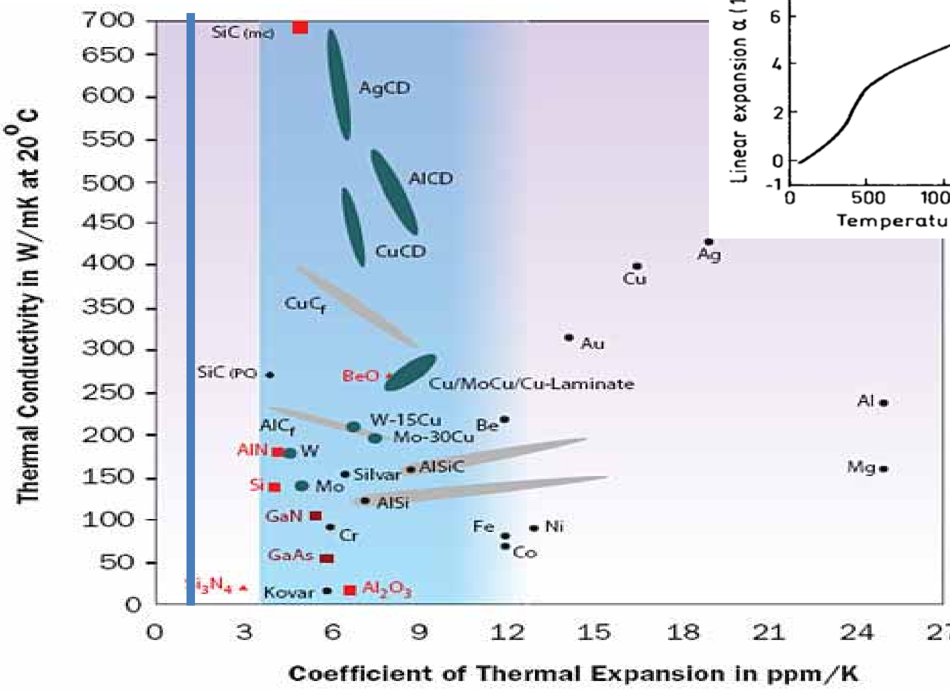
OR decreasing interface thermal resistance

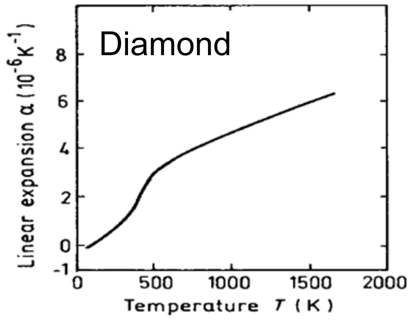


We validate all thermal simulations with Raman thermography measurements.

GaN-diamond stability

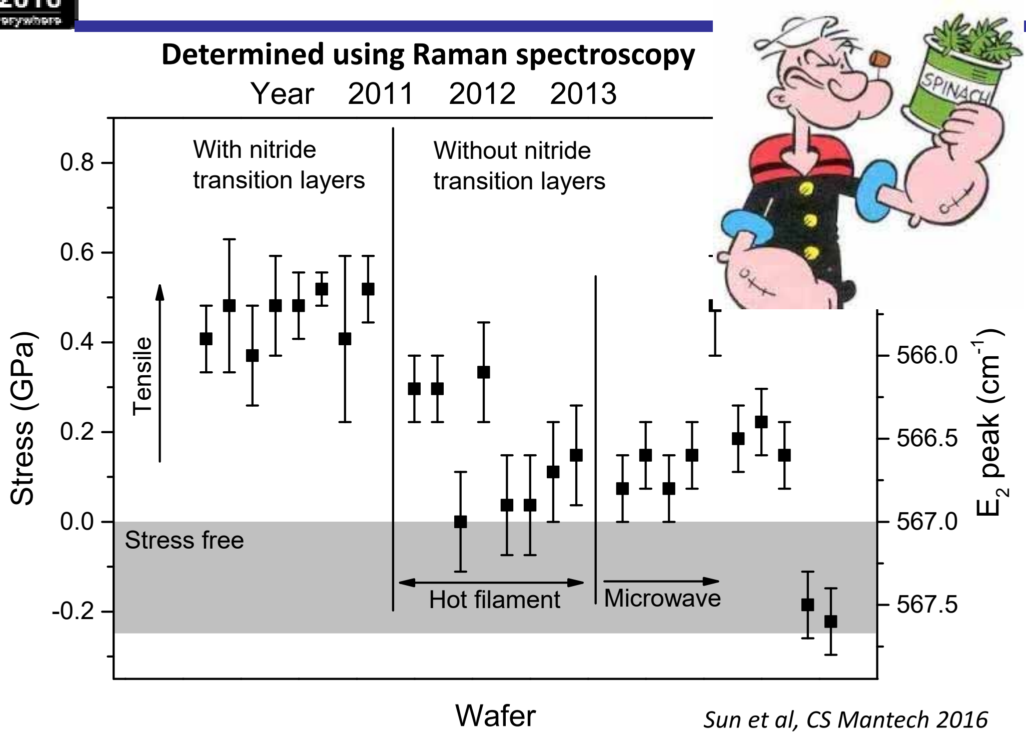
Coefficient of thermal exansion





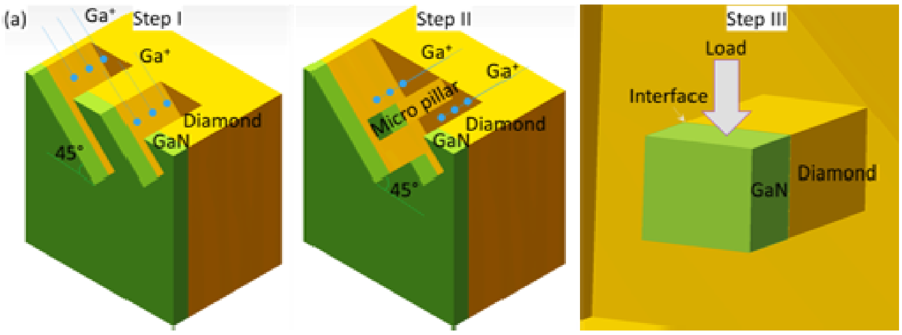
Stress in GaN layer

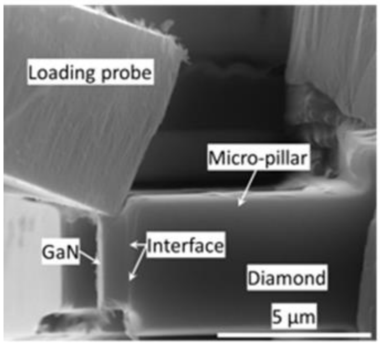
Determined using Raman spectroscopy



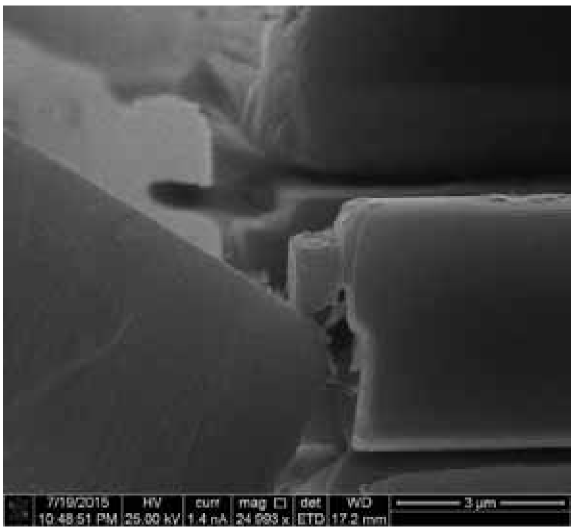
Sun et al, CS Mantech 2016

How to test for stability ?





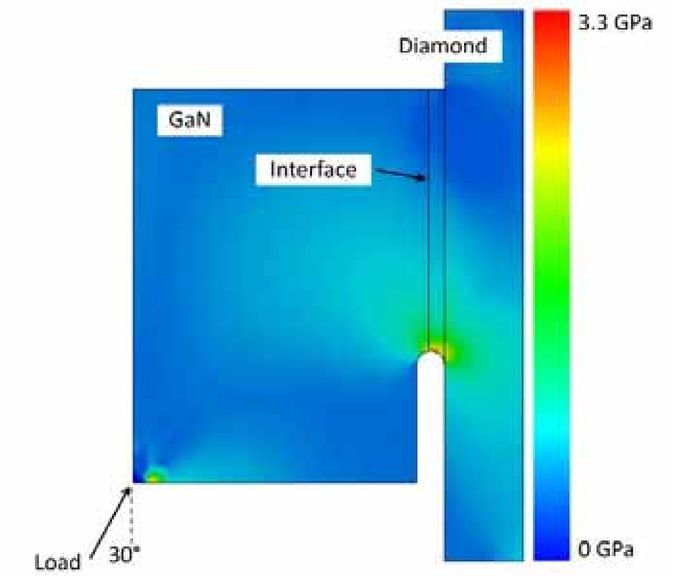
High mechanical stability



We try to cause fracture at the GaN-diamond interface

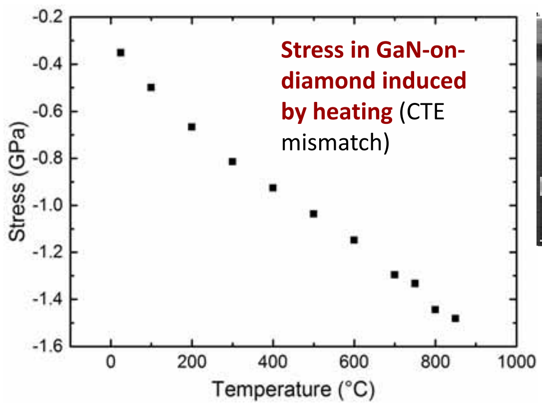
D. Liu et al, Appl. Phys. Lett., **107**, 251902 (2015).

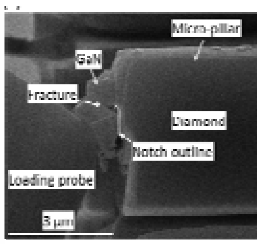
Estimation of interface strength



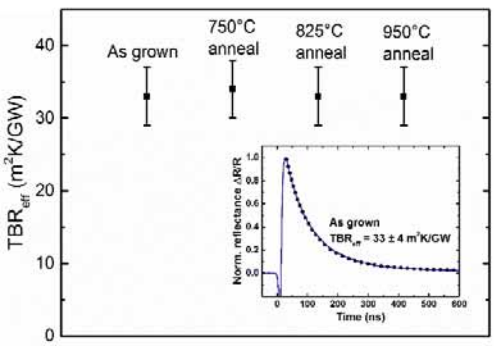
GaN layer fractures as >3 GPa; GaN/diamond interface fracture strength is much greater.

Thermomechanical stability





Fracture at > 3GPa



Good thermo-mechanical stability in the areas studied ie no change in the TBR after annealing.

Conclusions

- GaN electronics **main challenge** at present is its **heat sinking**.
- **Raman thermography** offers the opportunity **to quantify channel temperature**, and to identify and optimize thermal bottlenecks such as interfaces.
- **Raman thermography** enables **0.5µm spatial** and **10ns time resolution** thermal imaging in 3D, which can be improved further using **solid immersion lenses (SILs)**.
- GaN-on-Diamond HEMTs enable **3x improvement in power density**, however, require optimization in diamond thermal properties near the interface and of the interface itself.
- **Transient thermoreflectance** can be used for wafer mapping of thermal interfaces (before device fabrication) and for device thermal analysis.
- **High mechanical & thermo-mechanical stability of GaN-diamond interface** was demonstrated.

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Bahar Oner
Alexander Pooth
Maire Power
Ben Rakauskas
Will Waller
Yan Zhou

EPSRC Engineering and Physical Sciences Research Council
Innovate UK Technology Strategy Board
DARPA
EDA
esa
elementsix
and others

Wolfspeed™

Advances in GaN devices for high power, low cost applications

Simon M. Wood – Manager RF Business Development

October 5, 2016

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OUTLINE

- Company Overview
- Wolfspeed Product Portfolio
- Wafer material selection
- Packaging Choices
  - Metal-Ceramic vs. Plastic
  - Thermal modeling
  - Thermal coefficient of expansion and Die attach selection
  - Plastic overmold selection
  - Qualification and Reliability testing
- High power ceramic product examples
- Plastic packaged product examples
- Summary

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UNLOCKING VALUE AND ACCELERATING INVESTMENT AND INNOVATION

CREE

Power and RF Division

Wolfspeed

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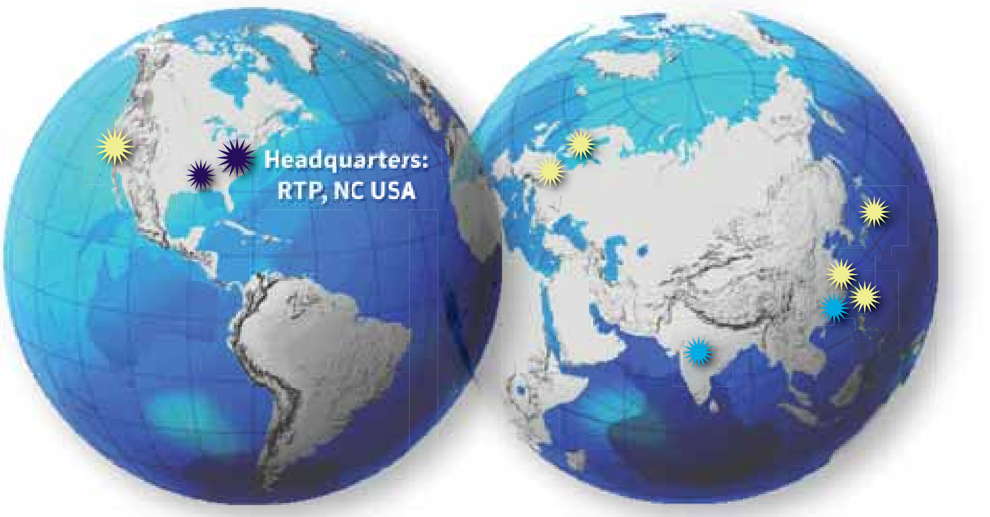
WOLFSPEED IS AN ESTABLISHED, GLOBAL, GROWTH COMPANY



- Wolfspeed
- Sales Offices
- Application Centers

Wolfspeed Facts

- $124M Revenue FY2015
- Double-Digit Growth
- Debt-Free Balance Sheet
- Growth Fueled Organically and Via Acquisition

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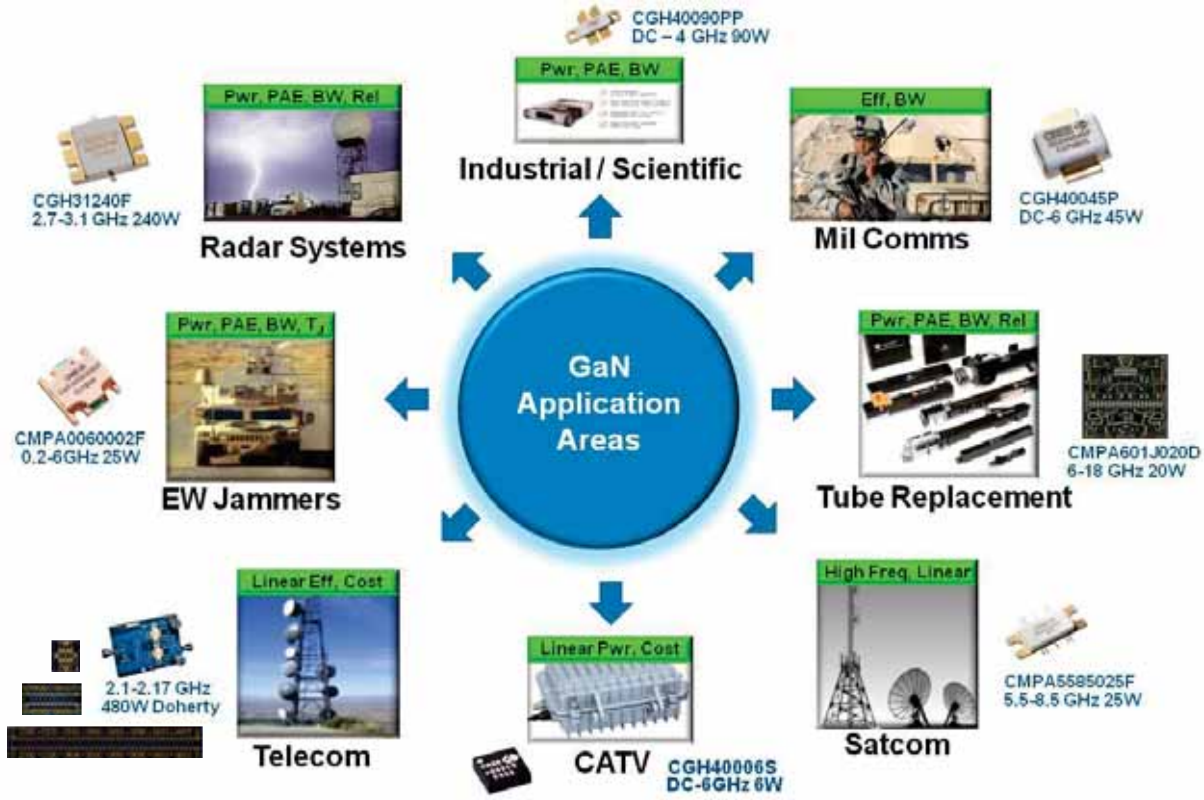
GaN PROCESS SUPPORTS MULTIPLE APPLICATION AREAS



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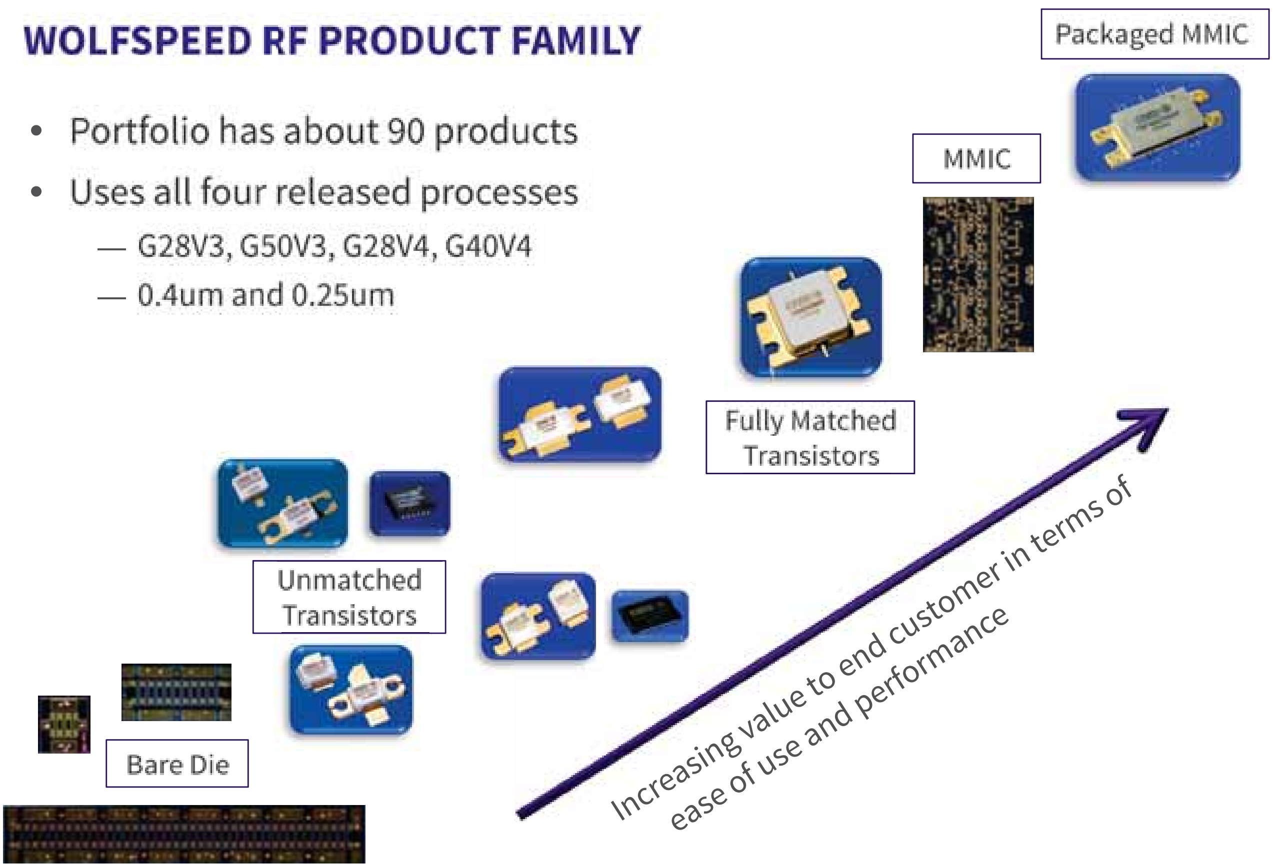
WOLFSPEED RF PRODUCT FAMILY

- Portfolio has about 90 products
- Uses all four released processes
  - — G28V3, G50V3, G28V4, G40V4
  - — 0.4um and 0.25um



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SEMICONDUCTOR WAFER CHOICES FOR GaN

Characteristic	Silicon Carbide	Silicon	Diamond
Thermal Conductivity	490 W/m-k	150 W/m-k	2200 W/m-k
Power Density	10 W/mm	0.3X SiC	3x SiC
Wafers Size	150mm	150mm	150mm
Cost	Medium	"Low"	High
Resistivity	High	• Doping for high resistivity increases wafer cost • Decreases with temperature	High
Maturity	> 15 years of volume production with 3 suppliers quoting MRL8	Epitaxy defect density is 10X compared with SiC	Low
Adoption	Wolfspeed, Sumitomo, Qorvo, Raytheon, Northrup, Integra, UMS, Mitsubishi, Toshiba	MA/Comm, Ohmmic	Qorvo, Raytheon (development only)

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PACKAGING CONSIDERATIONS

- GaN delivers higher RF power density (~10W/mm) at higher operating temperatures than traditional semiconductors
- Application
  - Radar → High power pulsed
    - Pulse width from 5 to 500 usec
    - Duty cycle from 2 to 20 %
  - ISM → Narrow RF bandwidth, high power CW, with high efficiency
  - Jammers / EW → Wide RF bandwidth, CW, with associated low efficiency
  - Telecommunciations → Backed-off linear, with high peak to average modulation
- High thermal dissipation requires high conductivity (k) die attach and heat spreader materials
- Coefficient of thermal expansion (CTE) increases with conductivity
- Cost vs. Thermal performance

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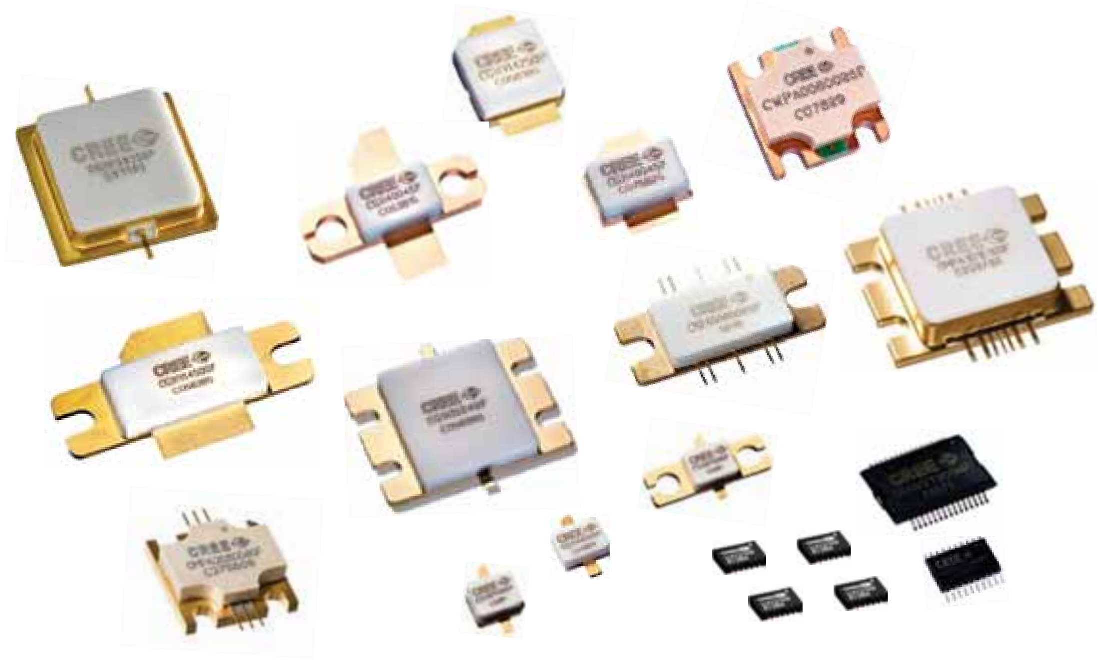
RF POWER PACKAGE EXAMPLES



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CERAMIC AIR CAVITY OR PLASTIC?

Air Cavity Ceramic

- Copper Tunsgten (CuW) and Copper Molybdenum (CuMo) composite metals provide moderate thermal conductivity with good CTE
  - CTE < 7 ppm/°C
  - k ~ 160 W/m-K
- Copper / Moly laminates provide a useful trade-off between thermal conductivity & CTE
  - CTE < 10 ppm/°C
  - k > 250 W/m-K
- Many open tool options
- Quick design cycle

Plastic Overmold

- Copper lead frames with high thermal conductivity but high CTE
  - CTE ~ 14 ppm/°C
  - k > 250 W/m-K
- High tooling costs ~ $400K
- Not many open tooled options for high power
- Low cost materials and manufacturing
- More challenging RF design medium
- Longer turn-time working with off-shore assembly and test companies (OSAT)

Note – Silicon and Silicon Carbide both have a CTE ~ 4 ppm/°C whereas Diamond is about 1 ppm /°C

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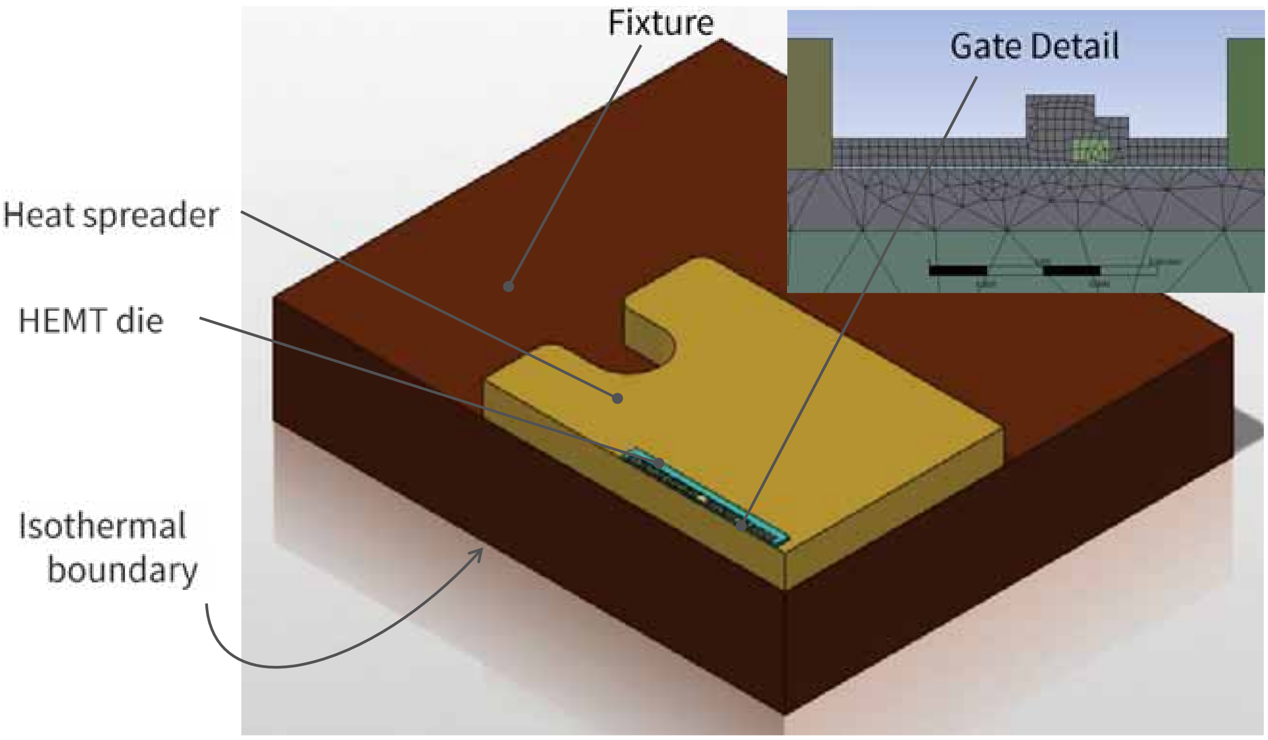
THERMAL MODELING GaN-ON-SiC PRODUCTS



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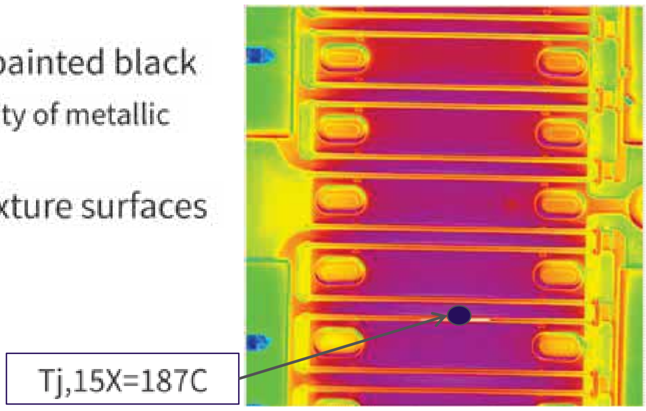
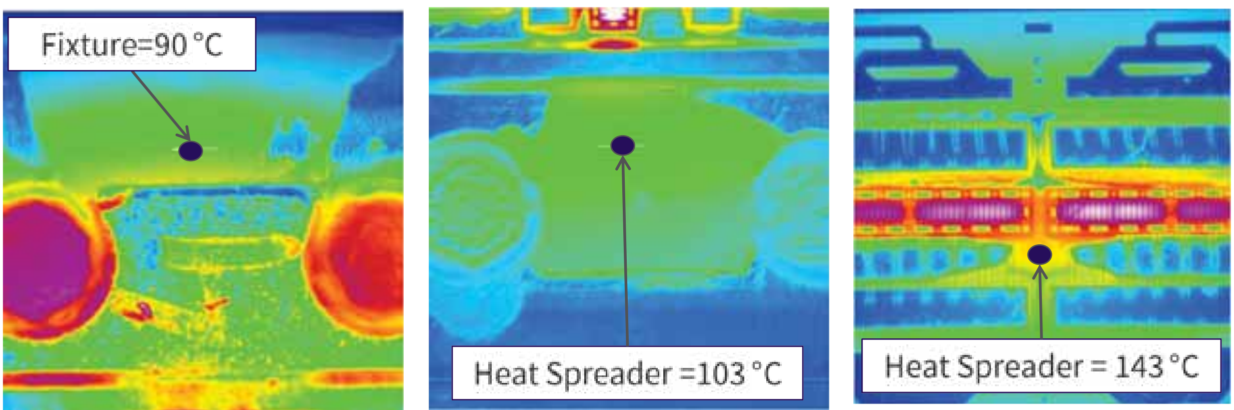
IR MEASUREMENT METHOD

- Fixture and heat spreader surfaces painted black
  - To alleviate concerns with IR emissivity of metallic surfaces
- 1X measurements of package and fixture surfaces
- 15X measurements of die channel
- IR stage temperature = 75 °C
- Power dissipation = 167 W





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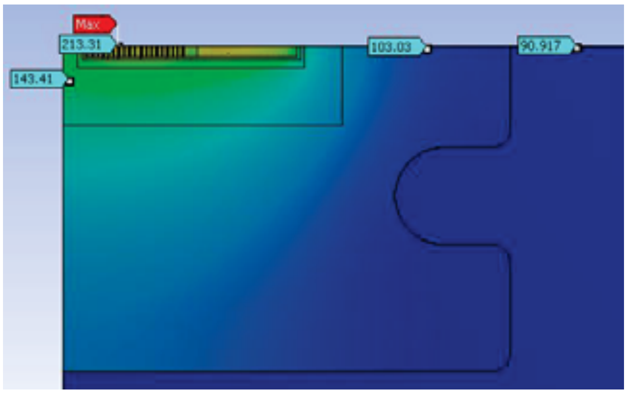
CALIBRATION AND VALIDATION OF THERMAL MODELS

- Thermal model is calibrated by
  - Adjusting the isothermal boundary temperature until the modeled fixture surface matches the IR measurement
  - Adjusting the package to fixture contact resistance until the Flange and Package Base surface temperatures match the IR measurements
- IR measurement of the die surface is averaged over a 5um spot size
  - Expected to be cooler than modeled peak T_j due to IR emissivity
  - Peak T_j can not be measured directly with IR since it is covered by a field plate

	Measured	Modeled
Fixture	90	91
Flange	103	103
Package Base	143	143
Tj, average (5um)	187	199
Tj peak	-	213



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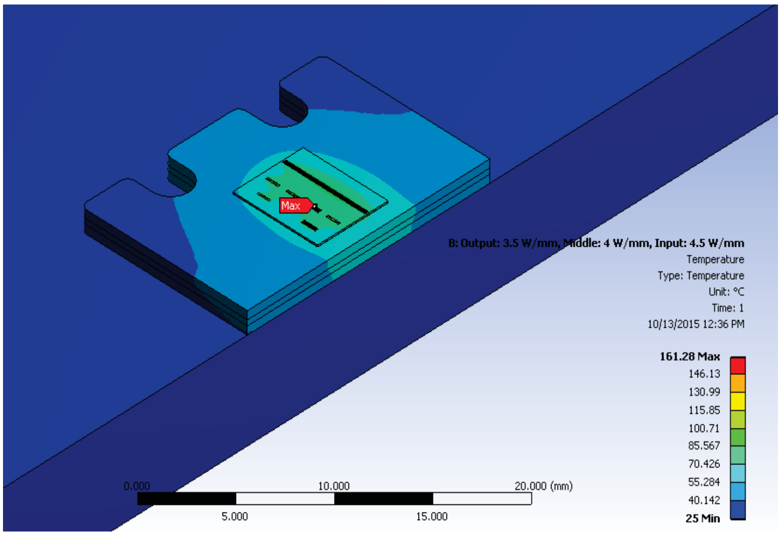
THERMAL SIMULATION OF A MULTISTAGE MMIC



Stage	Pdiss (W/mm)	Peak Tj (°C)	Rth (°C/W)
1	4.5	156	9.7
2	4.0	161	4.7
3	3.5	159	2.7

- Thermal design is a part of the RF design process
  - Power density and thermal resistance is stage specific
- Thermal simulation needs to include the entire thermal stack
  - CMC heat spreader, 0.25" inch aluminum base plate, and a 0.03 W/mm^2 interface resistance between package and base, representative of indium foil

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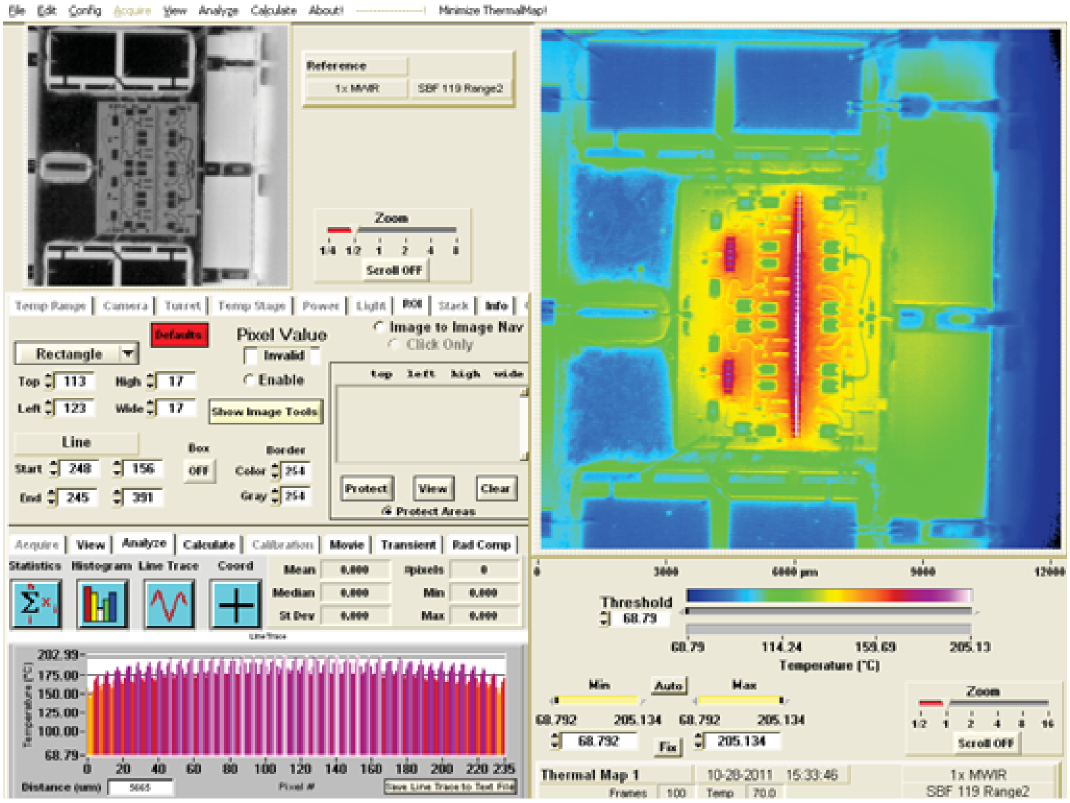
THERMAL IMAGE OF CMPA801B025F AT 5.5W/mm



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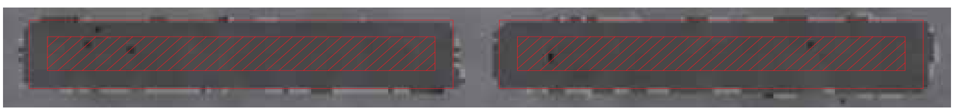
VALIDATION OF MATERIALS SYSTEM

- Mismatch between dissimilar materials leads to high mechanical stresses over temperature in the die attach interface
- Thermal cycle testing of die, die attach and heat spreader required
- High power die as used in CGHV31500F have a high aspect ratio
  - Die size → ~ 6mm x 1mm
  - High aspect ratio increases problem



Zero cycles

1000 cycles

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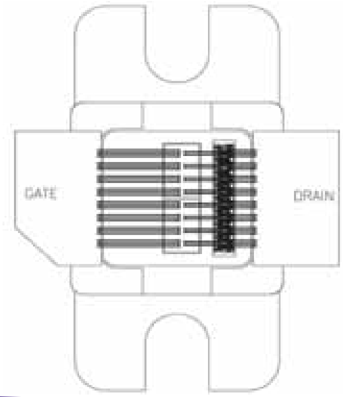
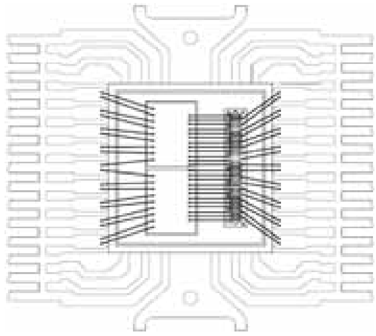
PLASTIC PACKAGE SELECTION

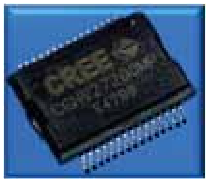
- Package outline availability
- Pad size must accommodate the die PLUS offsets required for assembly and reliability
- Design changes may be required to transition from air cavity to plastic due to added parasitics

Air cavity product



Product modified for open tool plastic





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DIE ATTACH FOR PLASTIC PACKAGING

- Eutectic solder
  - — Inadequate stress relief between SiC and copper LF
  - — Limited experience basis at OSATs (off-shore assembly and test)
- Standard Ag epoxy
  - — Limited thermal conductivity, k < 30 W/m-K
- Sintered Ag
  - ✓ Bulk thermal conductivity, k > 50 W/m-K
  - ✓ Modulus on par with Ag epoxy & much lower than AuSn
  - ✓ Low sintering temperature minimizes thermal history on LF
  - ✓ RoHS / REACh compliant

				Sintered Ag		
ITEM	**UNITS**	**AuSn**	**Ag Epoxy**	**Mfr A**	**Mfr B**	**Mfr C**
Bulk Thermal Conductivity	W/m-K	57	23	50	100	180
CTE	ppm/^{o}C	16	38	26	28	22
Modulus @ RT	Gpa	59	3.0	6.7	10	26

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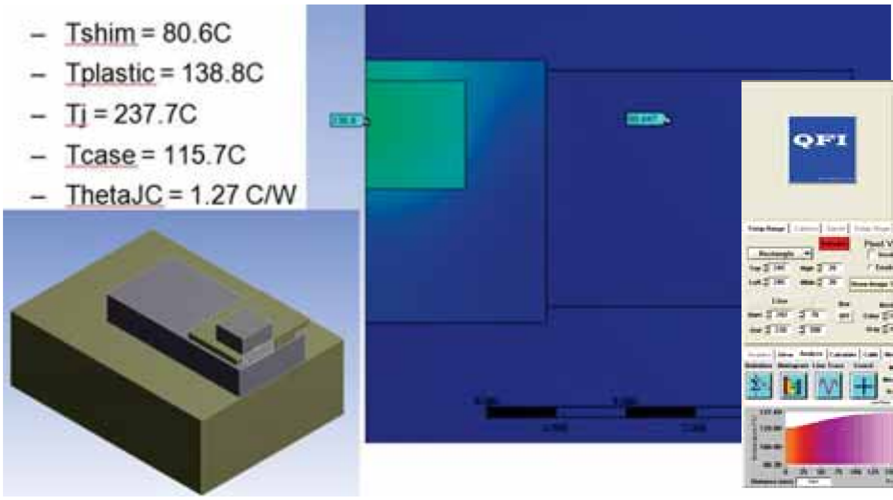
SINTERED SILVER THERMAL VIABILITY

- Sintered Ag thermally enables high power GaN in plastic
  - Tj,peak ≤ 225°C realized at Pdiss=125W steady state & Tcase = 105°C in 175mm² plastic pkg!

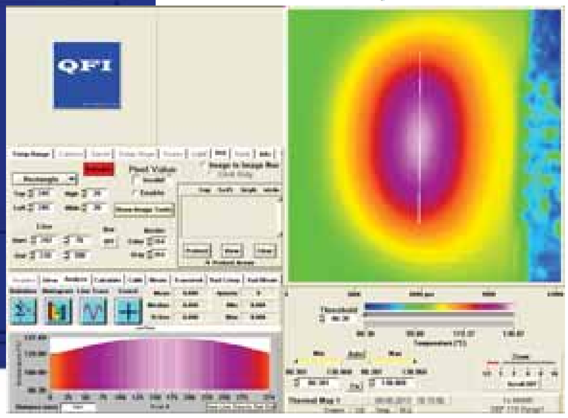
Modeled

- Tshim = 80.6C
- Tplastic = 138.8C
- Tj = 237.7C
- Tcase = 115.7C
- ThetaJC = 1.27 C/W



Measured

- Tshim = 81C
- Tplastic = 138C



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SINTERED SILVER THERMO-MECHANICAL VIABILITY

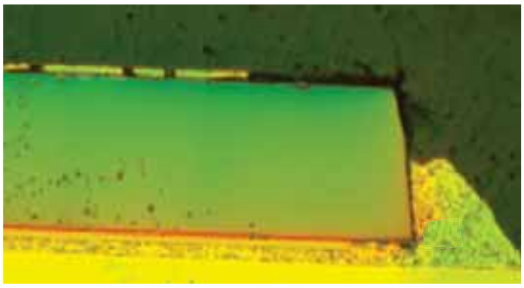
- Sintered Ag outperforms AuSn eutectic solder on copper
- 5mm x 1mm GaN-on-SiC die after TC -55 to +125C, 1000 cycles

.5 mil thk AuSn Zero TC

Nearly 100% delamination!

1000 TC

Sintered Ag after 1000 TC Negligible degradation!



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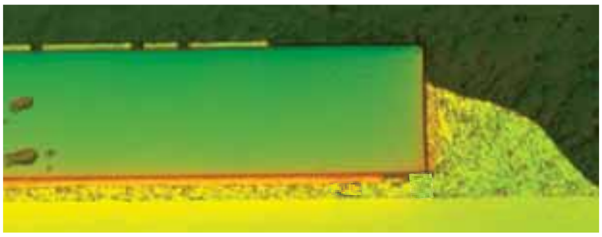
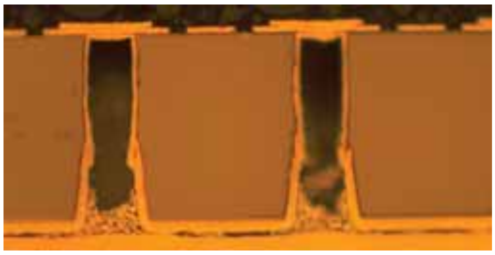
SINTERED SILVER PROCESS CONSIDERATIONS

- Sintered Ag bondline thickness (BLT)
  - — Needs to be small enough to meet thermal requirements
  - — And large enough to provide adequate stress relief between die and LF
- Need low voiding for good thermals & fillet for proper stress relief
- Die backside plated Au or Ag to improve adhesion to DA

Good BLT / Fillet



Insufficient BLT with large voids



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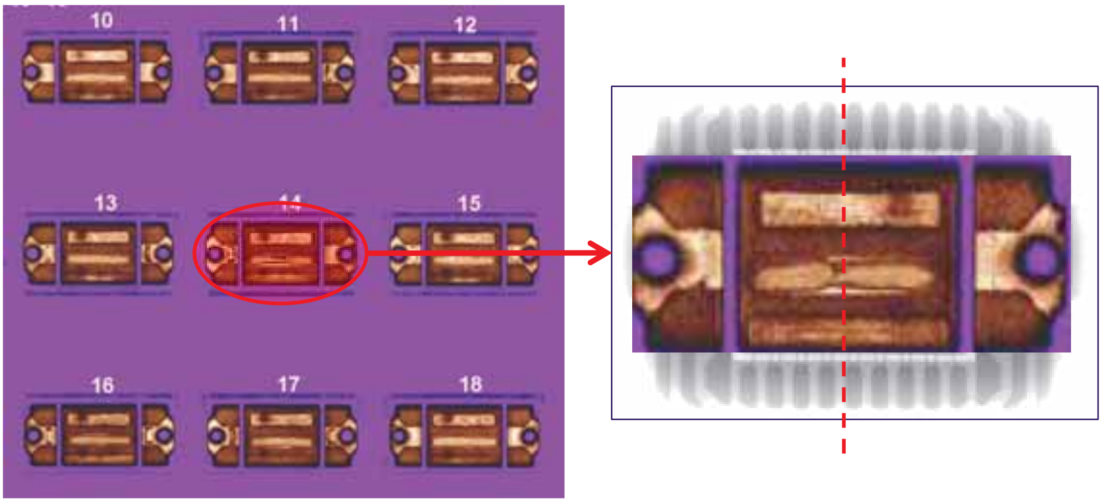
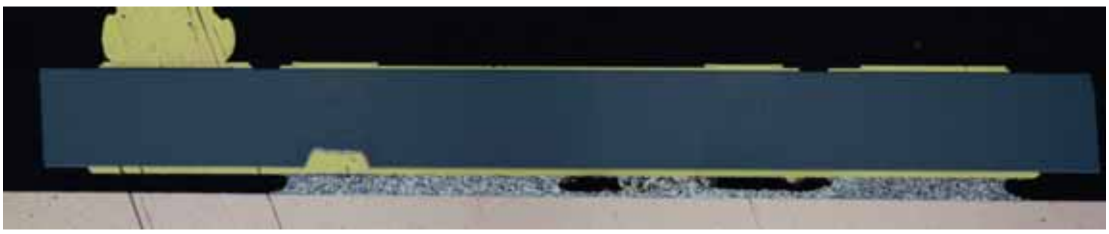
C-SAM AND X-SECTION ANALYSIS OF DIE ATTACH





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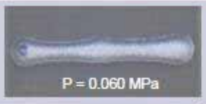
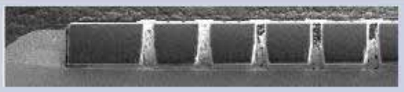
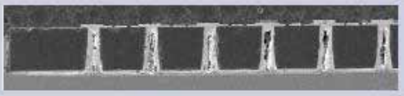
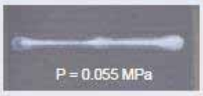
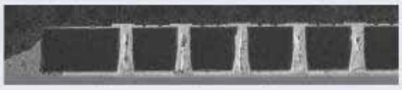
DIE ATTACH PROCESS OPTIMIZATION

Leg	Dispense Pattern	Nozzle Size	Actual Dispense Pattern Note: Pressure is baseline only, and may still vary per output response	Epoxy Coverage (Visual)	Sample Cross section Image
1	Single Line	0.2mm			
2	Double Y	0.2mm			
3	Double Y Plus	0.2mm			
Control	Single Line	0.4mm			

- All legs met requirements of 100% epoxy coverage and no epoxy voids (as measured by X-ray)
- Leg 1 has excessive voiding in the bond-line
- Leg 2 has best response

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TEMPERATURE CYCLING

Zero TC

500 TC

1000 TC

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PLASTIC OVERMOLD MATERIALS SELECTION

- Considerations for GaN overmold selection:
  - Thermal suitability for Tj = 225°C and weight loss at high temperature
  - Operating temperature range, Tg and resulting CTE stresses with LF, die and die attach fillet
  - Low modulus – compliant enough to handle CTE mismatch to LF
  - Strong adhesion to LF surface, die and die attach fillet
  - Low water absorption for MSL, HAST and THB compliance
  - Mold flow compatibility with selected LF

ITEM	UNITS	Mfr A	Mfr B	Mfr C	Mfr D
Tg	°C	250	190	175	120
CTE 1	ppm/°C	10	11	7	9
CTE 2	ppm/°C	60	50	34	40
Modulus @ RT	Gpa	15.5	15.5	18.5	23.5
Adhesion (Ag or Au) @ RT	Mpa	10	13.0	14.0	16.0
Moisture Absorption	%	0.64	0.35	0.22	0.13

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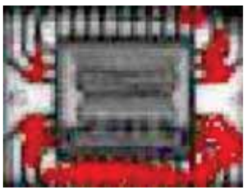
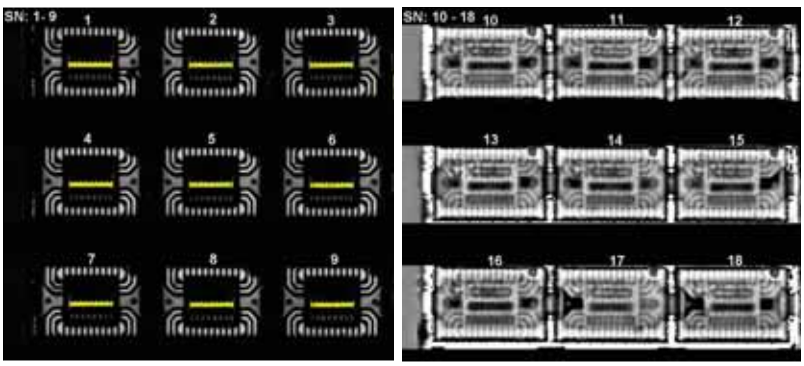
PLASTIC OVERMOLD PROCESS CONSIDERATIONS

- Mold temperature / pressure / flow should be tightly controlled to prevent wirebond sway and mold voids
- Post mold cure (PMC) temperature / time important for polymer cross linkage to yield expected Tg, modulus and adhesion

Good processing with no LF delam post-PMC



Improper processing with LF delam post-PMC



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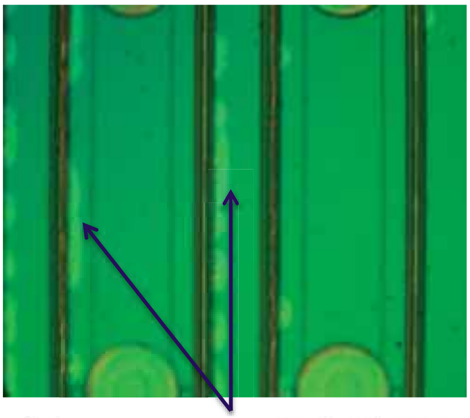
PLASTIC OVERMOLD RELIABILITY

- Impact of overmold selection – thermal cycle (TC)
- GaN-on-SiC die post TC -55 to +125C, 1000 cycles

Damage caused by high modulus mold compound

Field plate distortion



Delamination of passivation layer

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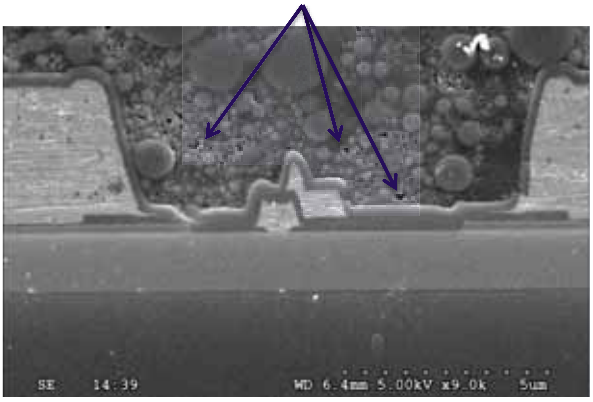
OVERMOLD PLASTIC PERFORMANCE AT ELEVATED TEMPERATURE

- High temperature operating life (HTOL) and High temperature storage life (HTSL)

Pitting of overmold around gate area post-HTSL

Overmold pitting



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QUALIFICATION TESTING

Test	Stress	Duration	Devices Sampled	Reference
High Temperature Reverse Bias (HTRB)	125 V_{DS}, -8 V_{GS} T_a = 125 °C	1000 hrs	75	MIL STD 883G Method 1005
DC High Temperature Operating Life (HTOL)	50 V_{DS}, 96W DC T_j = 225 °C	1000 hrs	75	MIL STD 883G Method 1005
Temperature Cycle (TC)	-55 °C to 125 °C 5 min soak	1000 cycles	75	JESD22-A104 Condition B Soak mode 2
Humidity (THB)	85°C/ 85% RH	1000 hrs	75	JESD
Accelerated Humidity Test (HAST)	135°C/ 85% RH	96hrs	75	JESD
Moisture Sensitivity (MSL)	Level 3 30°C/60% RH Soak 3X 245°C Reflow	192 hrs Soak	60	MSL3 J-STD-020

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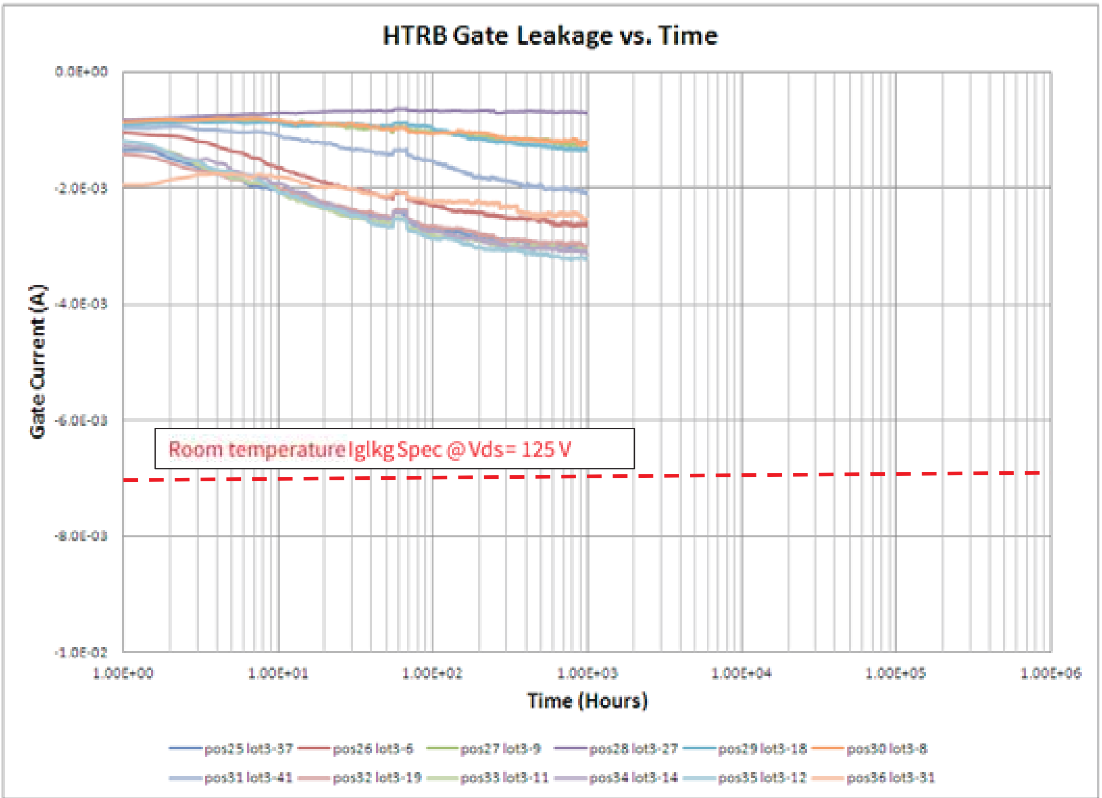
HTRB: V_{DS} = 125 V, V_{GS} = -8 V FOR 1000 hrs



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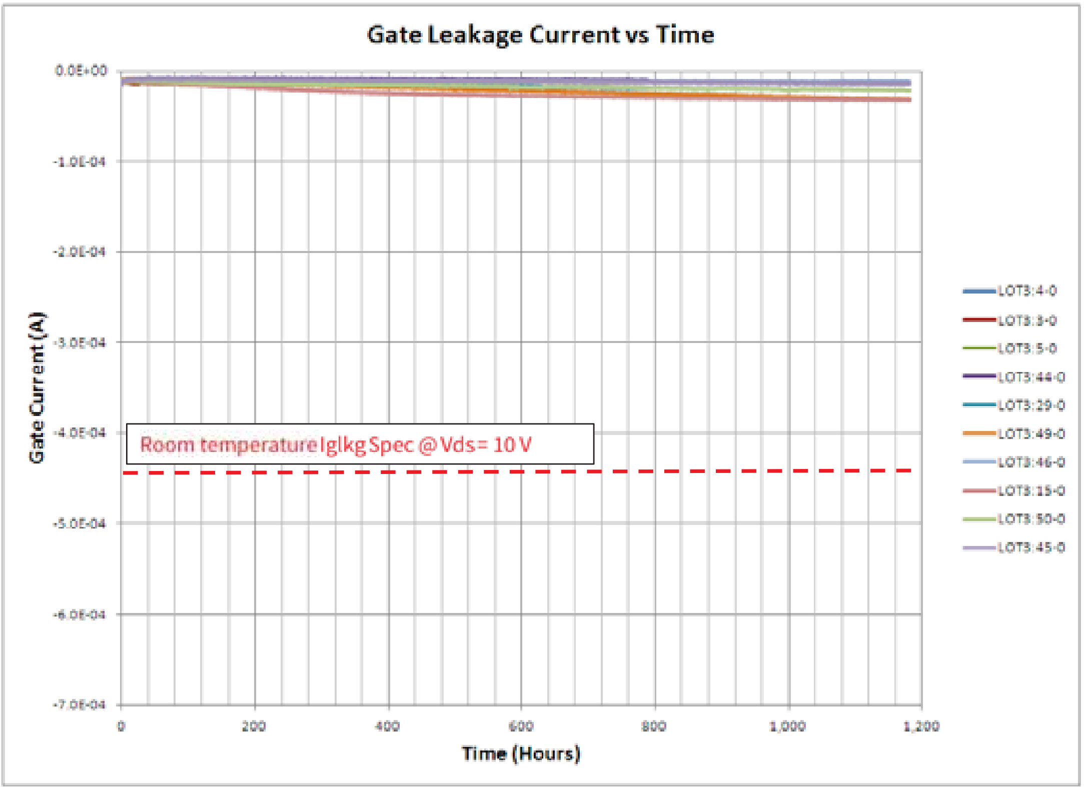
HTOL: 50V, P_{DISS} = 96 W (3 W/mm) FOR 1000 hrs



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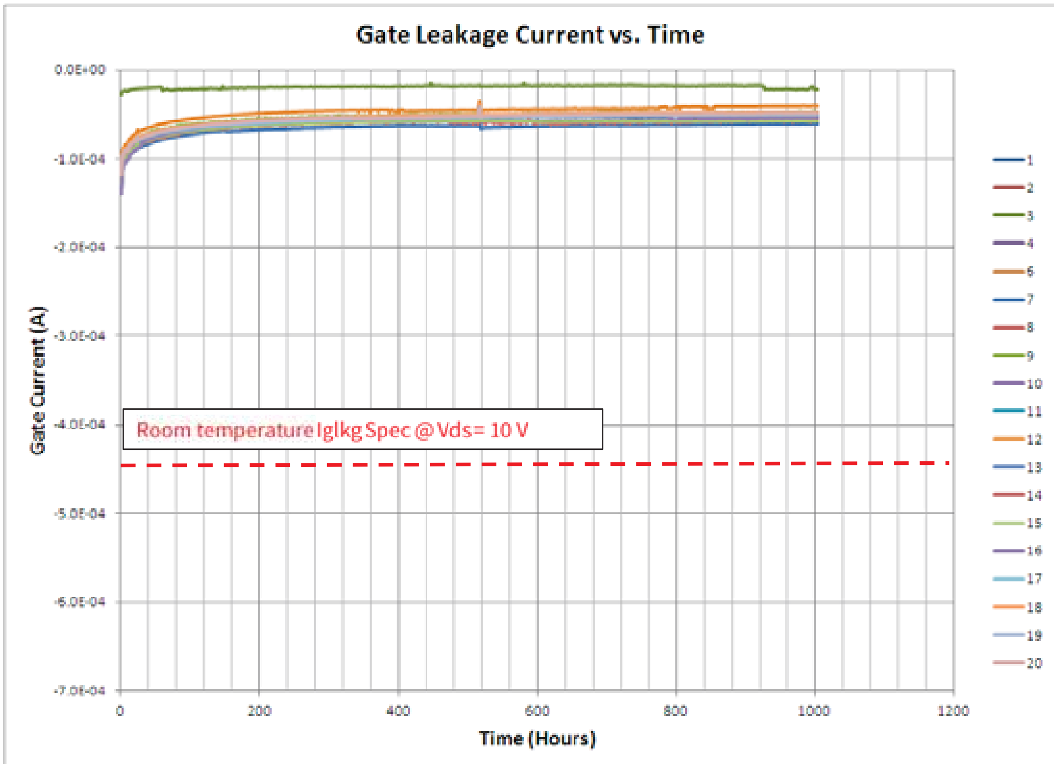
THB: 85 % RH, 85 °C FOR 1000 hrs



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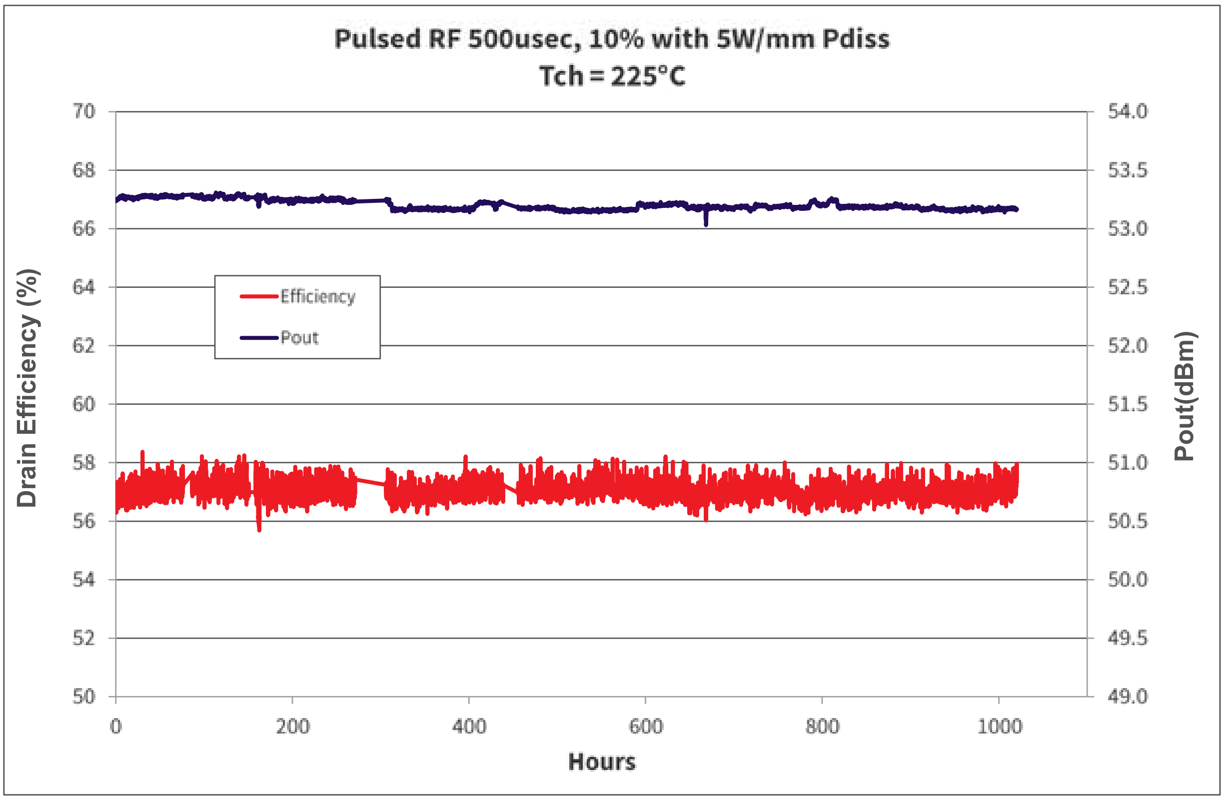
RF LIFE TEST



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HIGH POWER CERAMIC PRODUCTS

- Wolfspeed ceramic product portfolio has ~60 devices




CGHV14800
50V, 1000W Peak
L-Band

CGHV31500
50V, 700W Peak
S-Band

CGHV59070
50V, 90W Peak
C-Band

CMPA1D1E025
50V, 40W Peak
Ku-Band

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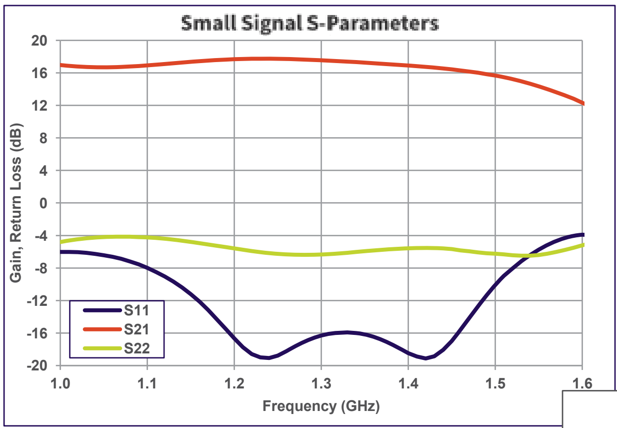
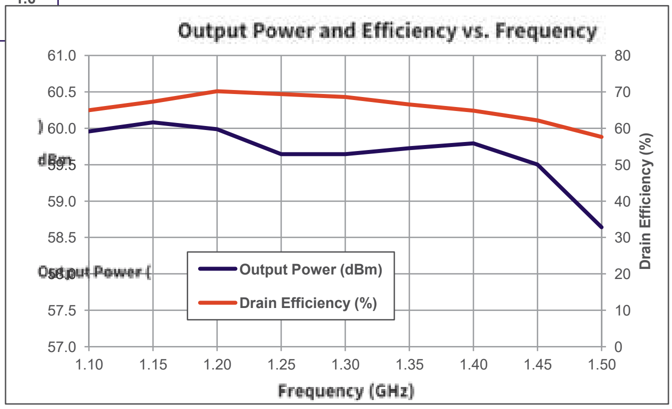
L-BAND 800W PULSED TRANSISTOR – CGHV14800





Features
Input and Output Matched
>15 dB Power Gain
950 W Peak Output Power
65 % Efficiency

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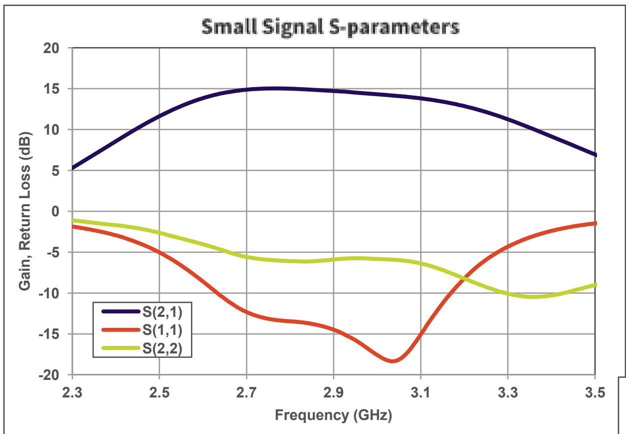
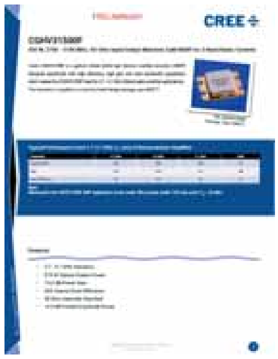
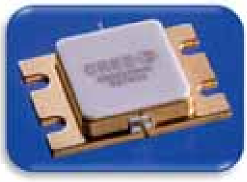
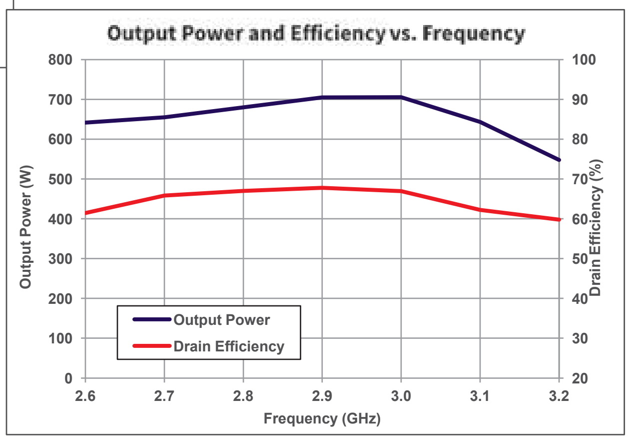
S-BAND 500W PULSED 50Ω TRANSISTOR – CGHV31500









Features
Fully Matched for ease of use
>13 dB Power Gain
>650 W Peak Output Power
60% Efficiency

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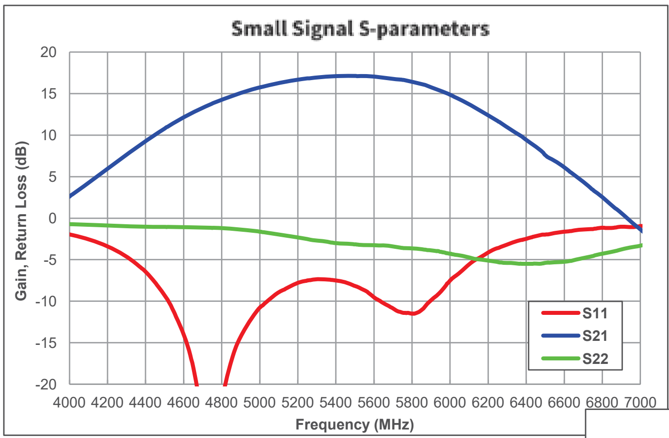
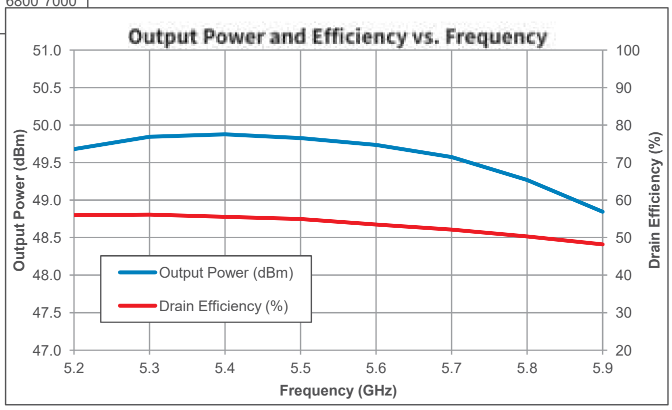
C-BAND PULSED & CW 70W TRANSISTOR – CGHV59070





Features

Input and Output Partial Match

14 dB Power Gain

90 W Peak Power

50 % Efficiency

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PLASTIC PACKAGED RF POWER TRANSISTOR PORTFOLIO


CGH40006S
28V, 6W CW

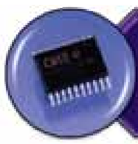

CGH27030S
28V, 30W Peak
4W Average

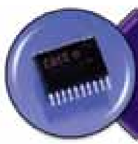

CGHV27015S
50V, 15W Peak
2W Average


CGHV27030S
50V, 30W Peak
4W Average


CGHV1F006S
40V, 6W Peak

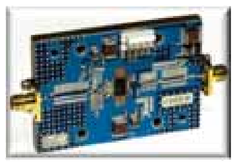

CGHV1F025S
40V, 25W Peak

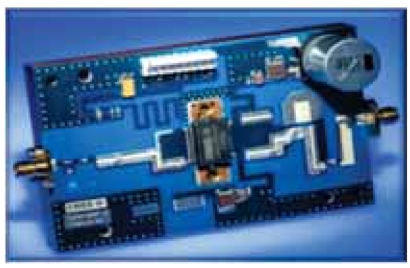

CGHV27060MP
50V, 60W Peak
10W Average


CGHV27030S
50V, 86W Peak
10W Average


CGHV09300MP
50V, 300W Peak
60W Average


CGHV22300MP
50V, 300W Peak
60W Average





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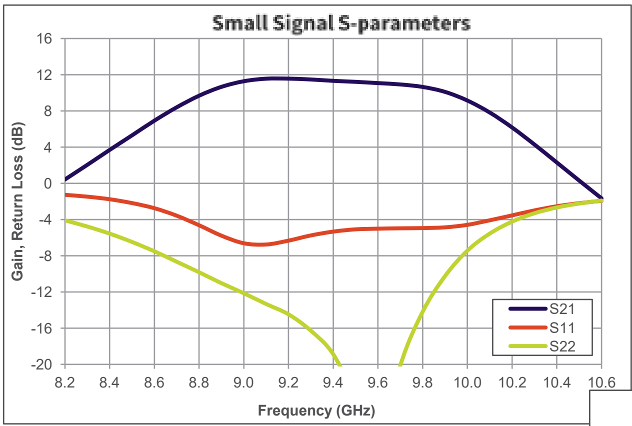
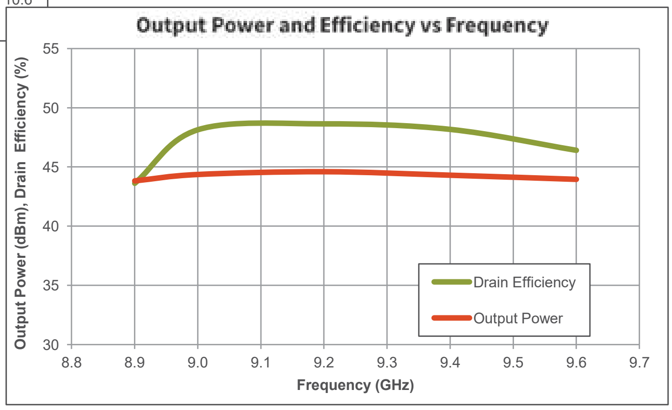
X-BAND 25W TRANSISTOR - CGHV1F025S





Features

Unmatched for flexibility

>11 dB Gain

25 W Peak Output Power

47 % Efficiency

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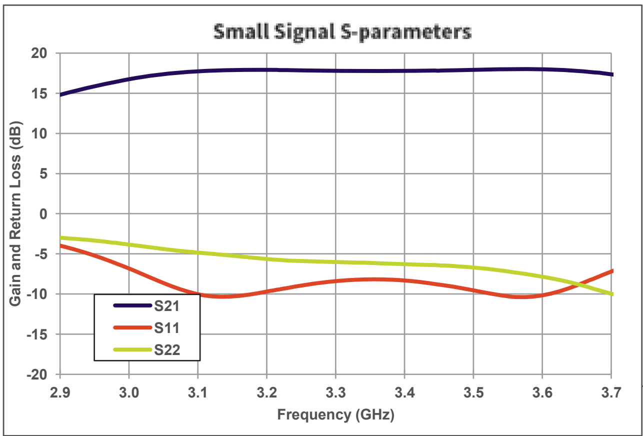
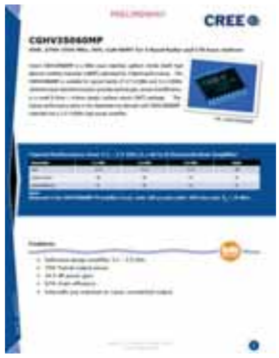
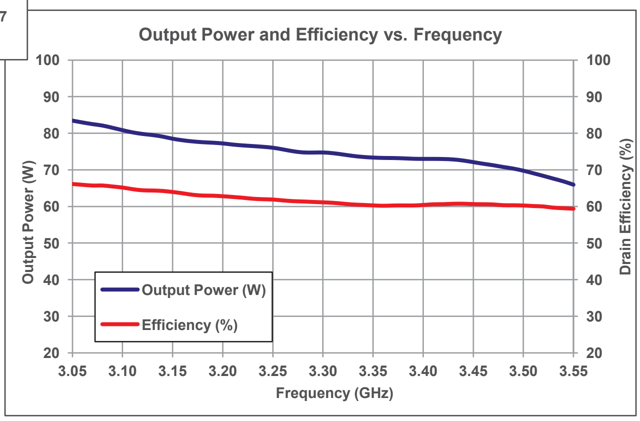
S-BAND 60W PULSED TRANSISTOR - CGHV35060MP







Features

Pre-matched for high performance

>14 dB Power Gain

75 W Peak Output Power

60 % Drain Efficiency

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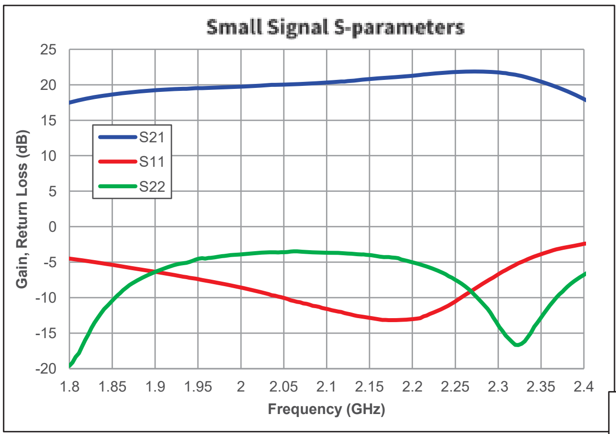
S-BAND 300W TRANSISTOR - CGHV22300MP



Features

18 dB Linear Gain

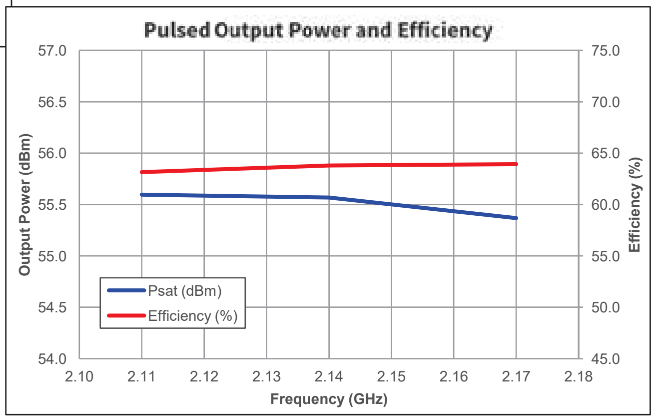
60 W Average Output Power

32 % Efficiency

-35 dBc Linearity

350 W Peak Power

63 % at Peak Power



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WOLFSPEED STATE OF THE ART PACKAGING

Package Type	RF Power (W)	RF Power Density (W/cm²)	Power Dissipated (W)	Dissipated Power Density (W/cm²)	Application
Ceramic / CMC CGHV31500	700	250	330	120	S-Band Pulsed Radar 500 usec, 10%
Ceramic / CPC CGHV14800	**1000**	500	540	**270**	L-Band Pulsed Radar 5 usec, 5%
Ceramic / CMC	100	115	110	125	<2 GHz CW
QFN CGHV1F025	25	210	30	**250**	X-Band Pulsed Radar 100 usec, 10%
QFN CGH27030	30	250	10	83	Milcom CW / Linear
TSSOP CGHV27060	80	280	47	165	<2.7 GHz CW / Linear
TSSOP CGHV35060	75	260	50	175	S-Band Pulsed Radar 300usec, 20%
PSOP CGHV22300	**350**	350	205 (125)	**205** **(125)**	Pulsed 100usec, 10% (Backed-off Linear)

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SUMMARY

- Industry standard substrate choice for GaN RF power devices is SiC
- Package choice has to be application specific
- Highest single ended power density demonstrated in Air Cavity Ceramic package
- Plastic packaged 300W products with excellent RF performance
- Plastic packaged 25W device at X-band
- Plastic packaging can offer reliable, high performance at lower cost

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Cost effective GaN HEMT developments with appropriate thermal transfer

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Outline

1. Fundamentals
2. Thermal Study of Substrate
3. Thermal Design (GaN for Radar)
4. Thermal Design (GaN for Base Station)
5. Summary

History of Sumitomo GaN HEMTs

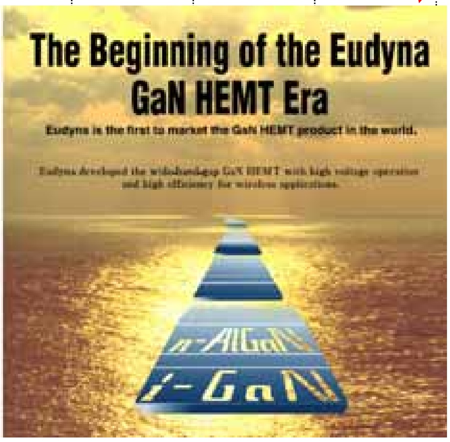
-2000 2003 2004 2005 2006 2007 2008 2009 2010 -

Fujitsu, Fujitsu Laboratories → ***Eudyna Devices*** → ***Sumitomo Electric Device Innovations***

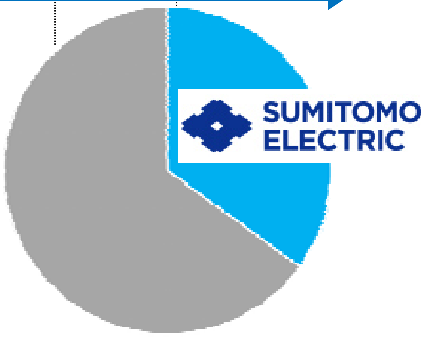
Development Start

Engineering Sample Release

Mass-production



- #1 Volume leader in RF high power GaN
- We strive for
  - Performance
  - Quality
  - Reliability
  - Cost
  - Capacity



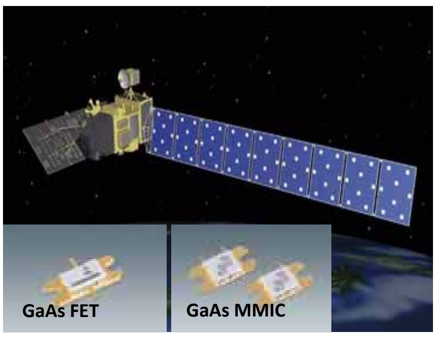
2013 GaN Market Share

above 5W below 4GHz Source: ABI Research 2014

Microwave Device Products

【Mobile Base Station】

【Satellite】



【Automotive Radar】

【Radio Link】

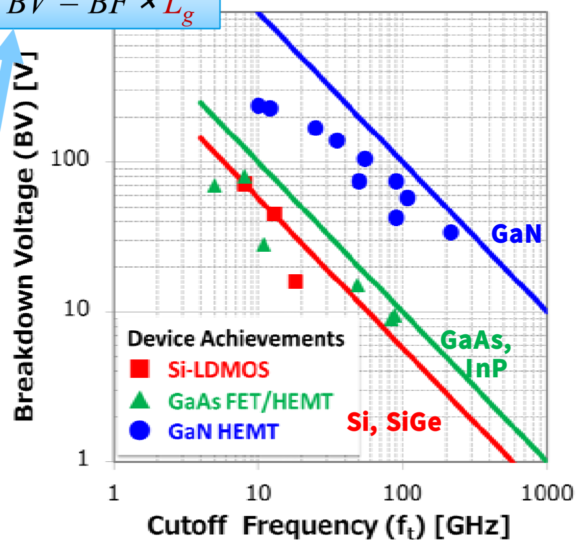
【Radar】

Why GaN ?
Johnson's Figure of Merit

Johnson's FoM $= f_t \times BV$
$= v_s / 2\pi \times BF$

Material	Si	GaAs	SiC	GaN
Bang Gap Energy (eV)	1.1	1.4	3.2	**3.4**
Critical Breakdown Field (MV/cm)	0.3	0.4	3.0	**3.0**
Thermal Conductance (W/cm/K)	1.5	0.5	**4.9**	1.5
Mobility (cm^2/V/s)	1300	6000	600	**1500**
Saturated Velocity (*10^7 cm/s)	1.0	1.3	2.0	**2.7**

$BV = BF \times L_g$



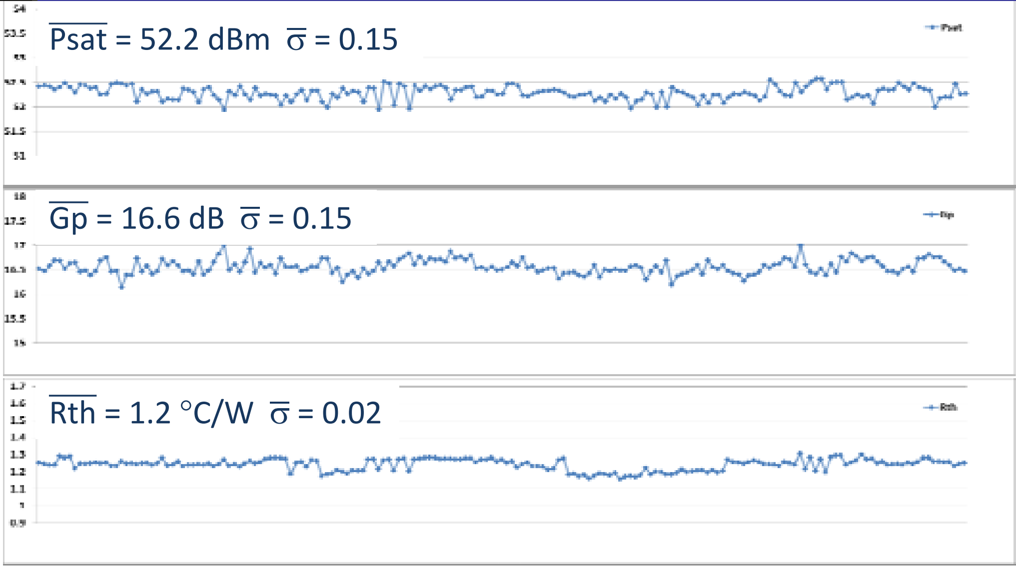
$f_T = v_s / (2\pi L_g)$

Cost Effective Design,
Focused on Thermal Transfer

- Chip cost is determined by ...
  - Wafer process cost and yield
  - Maximum channel temperature design

- Maximum channel temperature is determined by...
  - Reliability of the device technology
  - Thermal conductance of material (on-SiC, on-Si)
  - Chip pattern layout
  - Operating condition
    (Thermal dissipation ↔ Efficiency)

Yield of GaN HEMT Wafer Process



BTS GaN HEMT 2.7GHz 160W, n = 9000 pcs, 181 lots, σ = lot average

GaN HEMT wafer process has been refined, through over 10-years mass production.

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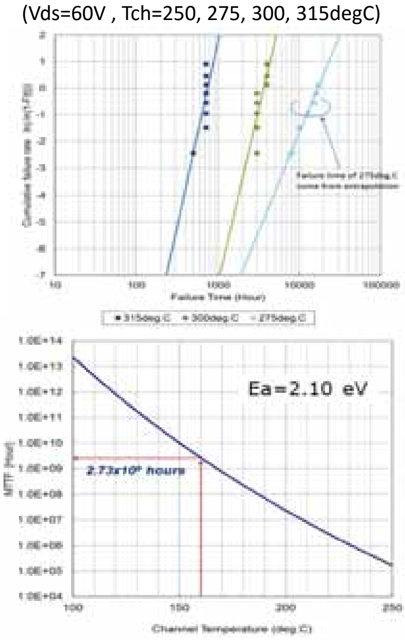
Reliability of GaN HEMT

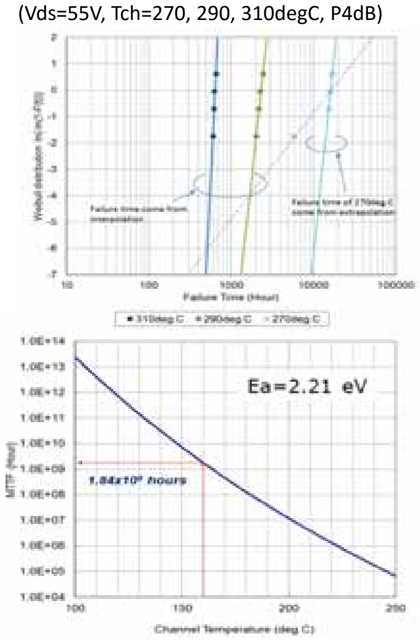
DC-HTOL test

(Vds=60V , Tch=250, 275, 300, 315degC)

RF-HTOL test

(Vds=55V, Tch=270, 290, 310degC, P4dB)

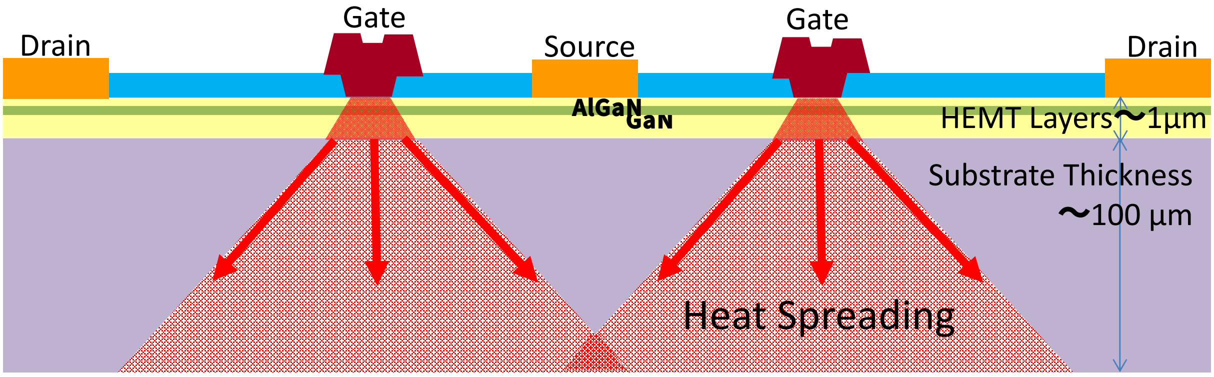




K.Osawa et.al, " Over 74% Efficiency, L-Band 200 W GaN-HEMT for Space Applications ," EuMC2016.

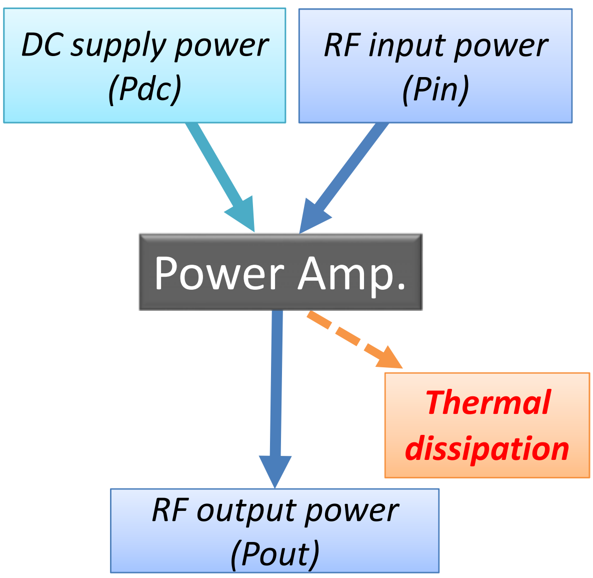
Material vs. Thermal Design

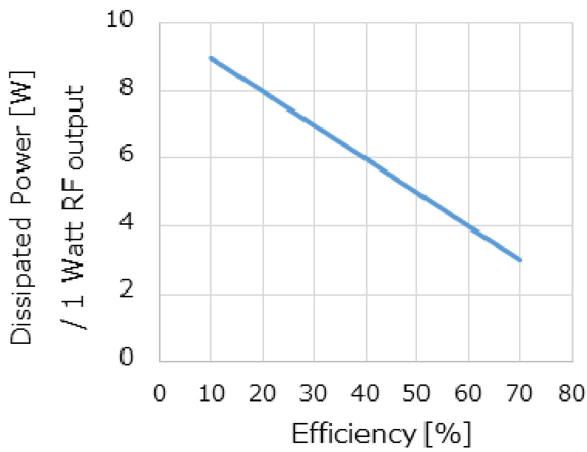
➢ Parameters, related to thermal design ;
  - Thermal conductance of substrate material (SiC:4.9 Si:1.5 [W/cm・K])
  - Substrate thickness (Typical thickness is ～100 μm)
  - Gate to gate pitch (Wide pitch improves the degree of heat spreading)



Thermal Design vs. Efficiency

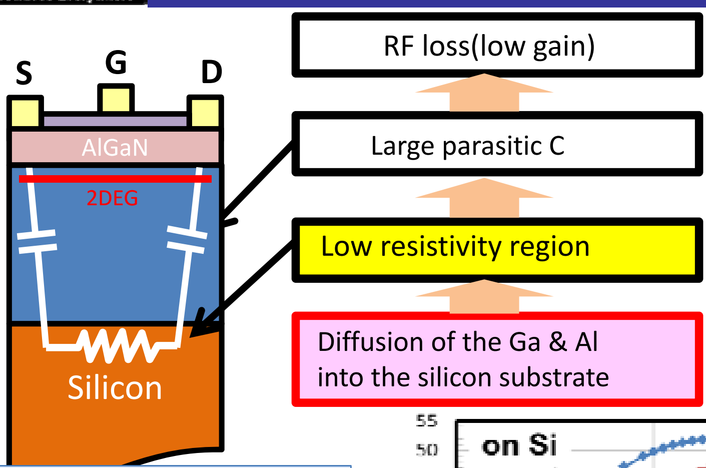
Thermal Dissipation = Pdc - Pout + Pin
= Pdc × (1 − Power-Added-Efficiency)

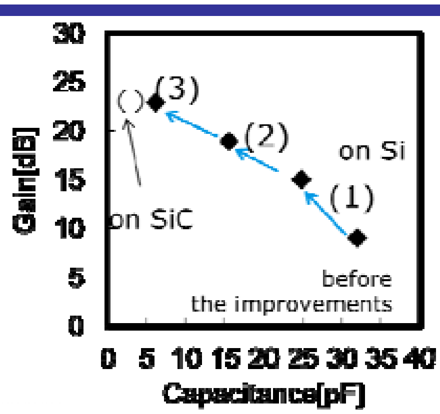




Outline

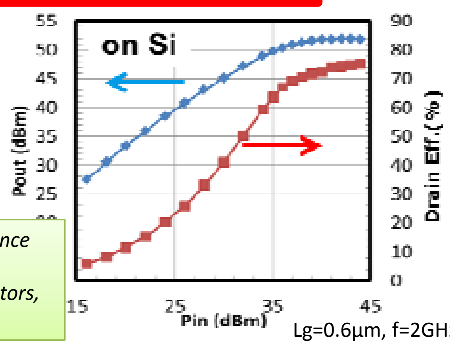
Case Study of GaN on-Si ～RF Performance

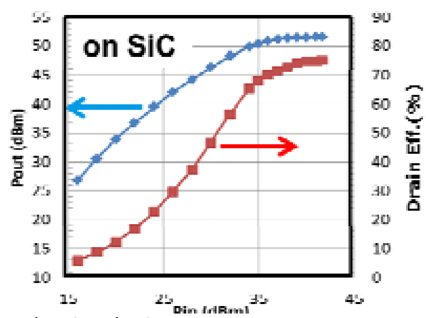




GaN HEMT on-Si realize comparable performance to GaN on SiC.

I. Makabe et al.," Improvement of RF performance of GaN-HEMT on silicon substrate,"Proc. International Workshop on Nitride Semiconductors, No. TuEP12, Wrocław, Poland (Aug. 2014)

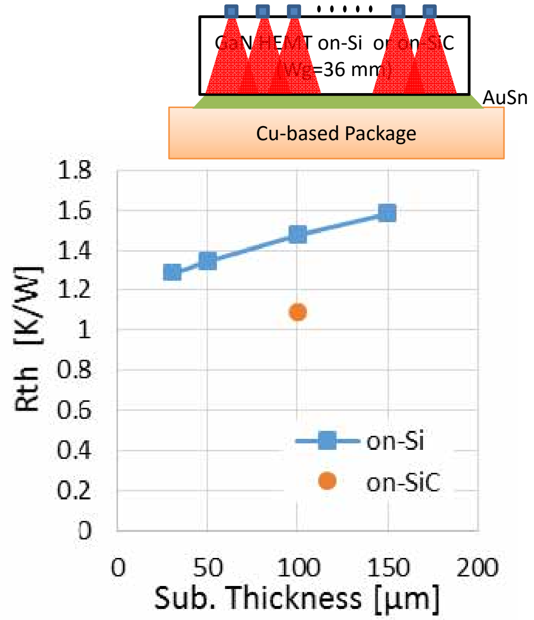




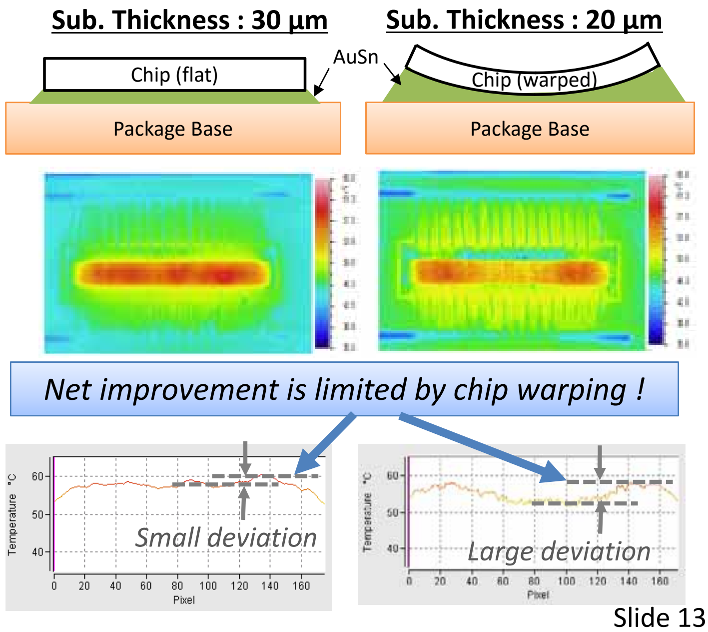
Lg=0.6µm, f=2GHz Vds=50V, Idq=0A

Case Study of GaN on-Si
〜Thermal Design (Sub. Thickness)

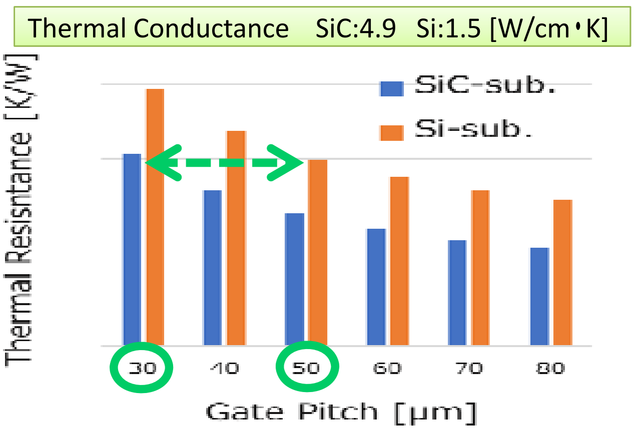
1. Simulated Thermal resistance is not comparable, even in 30 μm thickness.

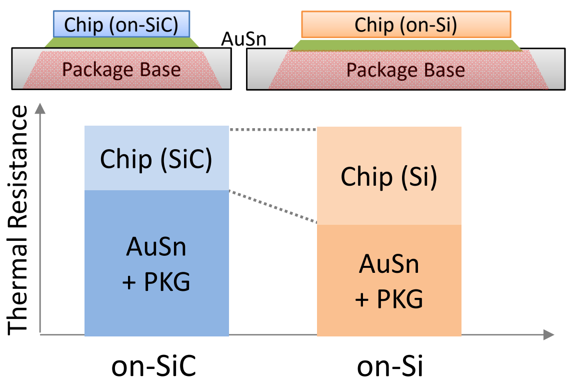


2. Excessive thinning causes chip warping @ GaAs MESFET



Case Study of GaN on-Si
〜Thermal Design (Gate Pitch)

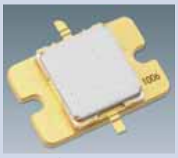
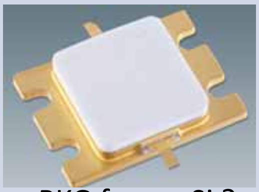
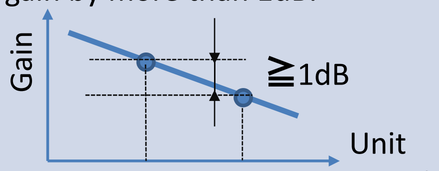




- Thermally equivalent pitch of GaN on-Si is 1.6 times of GaN on-SiC.
- SiC substrate cost used to be several times higher to the wafer process cost. In such cost structure, GaN on-Si was a reasonable solution.
- It should be noted the 1.6 times chip size increases “net wafer process cost” of GaN on Si
- The power density of GaN HEMT has been increasing. It used to be 〜5 W/mm, but now reaches to 〜10 W/mm. Higher power density favors better thermal conductance material.

Case Study of GaN on-Si ～Thermal Design (Chip Stretch)

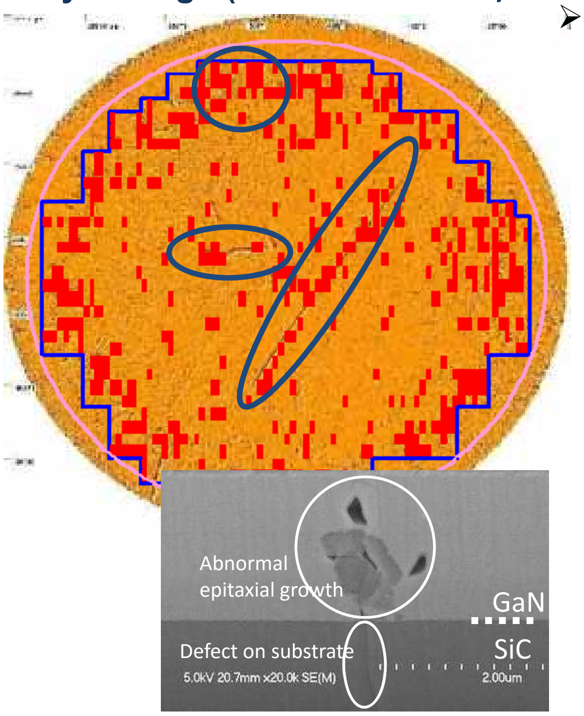
Two options to realize thermally equivalent GaN on-Si

	Option.1 (Lateral Stretch)	Option.2 (Vertical Stretch)
on-SiC		
on-Si		
Effect	- Larger PKG is required for on-Si chip.  PKG for on-SiC  PKG for on-Si ?	- Larger unit finger increases gate resistance, which degrades the gain by more than 1dB. 
Judgement	Total cost strongly depends on PKG price.	Trade-off issue arises (vs.gain).

GaN on-SiC is the best solution at present, judging from both cost and RF property.

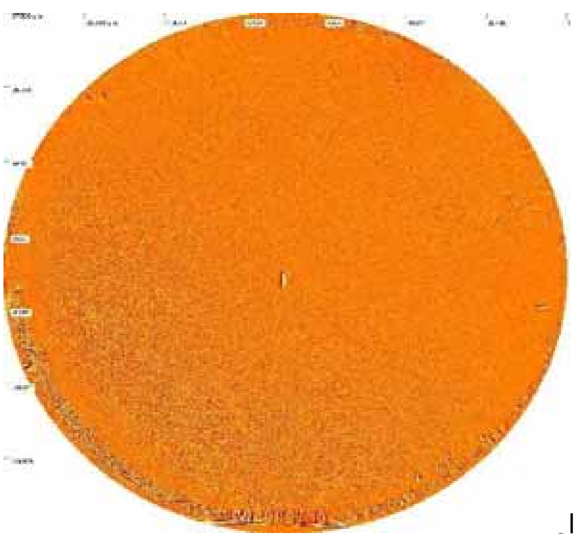
In addition… ～SiC Quality Improvement

10 years ago (Surface Defects)



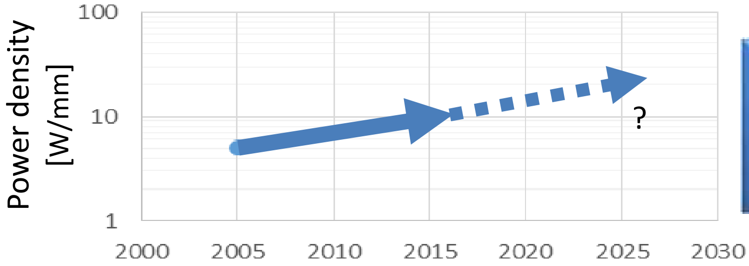
- SiC quality was one of the issues to be solved.
- The current SiC has realized smooth surface, and it contributes to the drastic improvement of the GaN on SiC cost structure.

Current SiC (Drastically Improved)



Prospect of Substrate Material

- Power density of GaN HEMT have been increased, and will be continued.
- The benchmark of GaN on Si vs. SiC indicates the availability of GaN on diamond.



Higher power density favors better thermal conductance material.

	2005	2016	2025
on-Si	- RF-loss elimination required	- Thermal limitation - No more cost effective	--
on-SiC	- Expensive & many defects - Chip selection needed	- Most promising	- Will be most promising - Thermal design may be critical @ >20W/mm
on-diamond	--	- Similar to early stage SiC ?	- Competitive @>20W/mm - Quality & cost required

Outline

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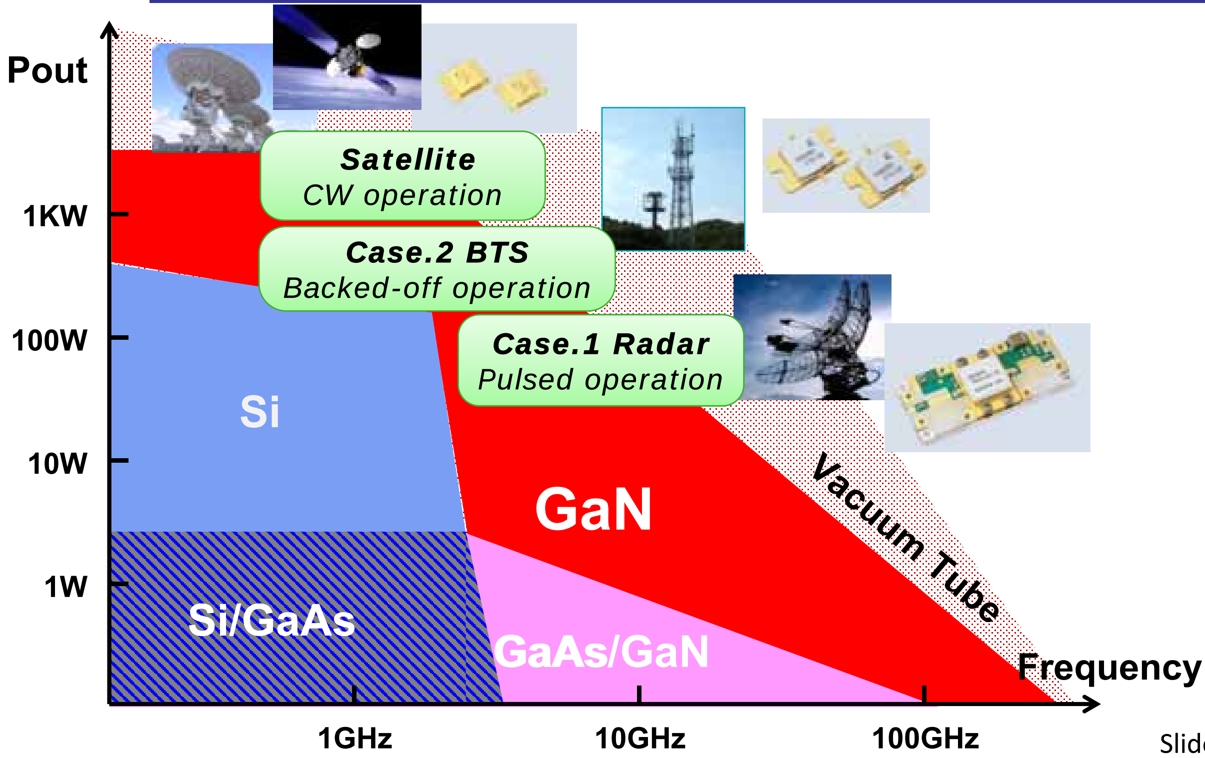
4. Thermal Design (GaN for Base Station)
5. Summary

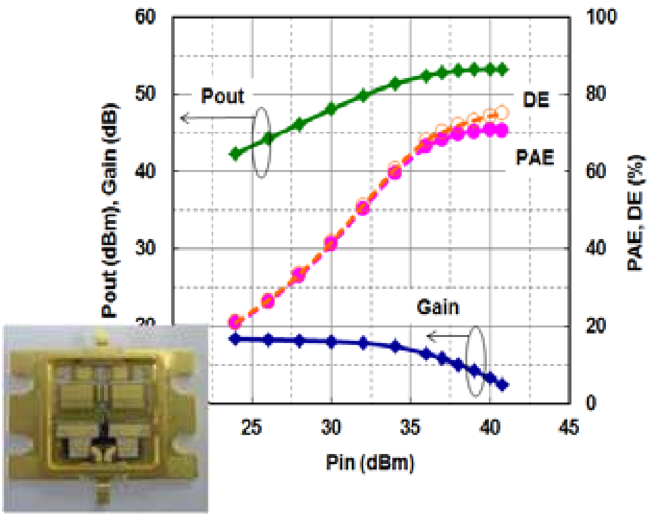
Output Power vs. Frequency



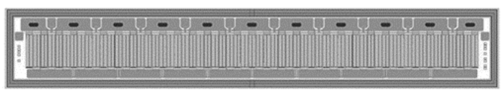
Satellite Application (CW-operation, as a reference)

Over 74% Efficiency, L-Band 200W GaN-HEMT for Space Applications

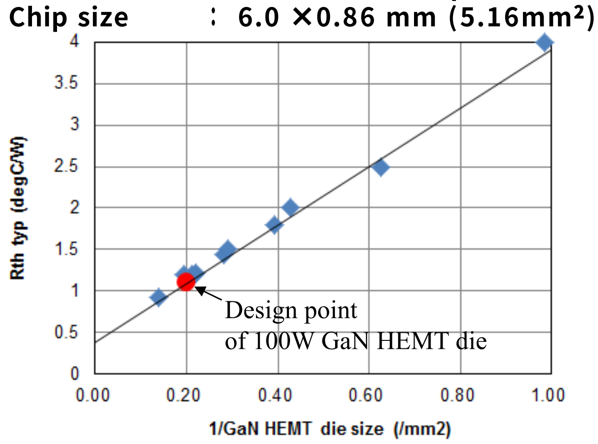
Ken Osawa, Hiroyuki Yoshikoshi, Atsushi Nitta, Tsuneyuki Tanaka, Eizo Mitani* and Tomio Satoh



K.Osawa et.al, " Over 74% Efficiency, L-Band 200 W GaN-HEMT for Space Applications ," EuMC2016.

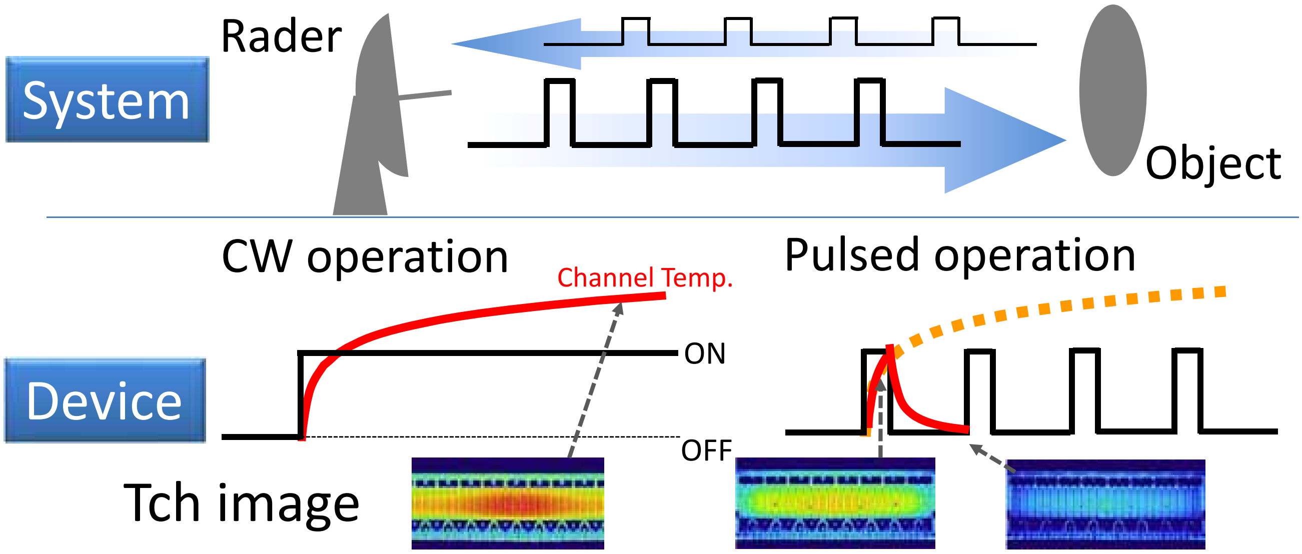


Gate width : 24 mm × 2 chip
Chip size : 6.0 ×0.86 mm (5.16mm²)



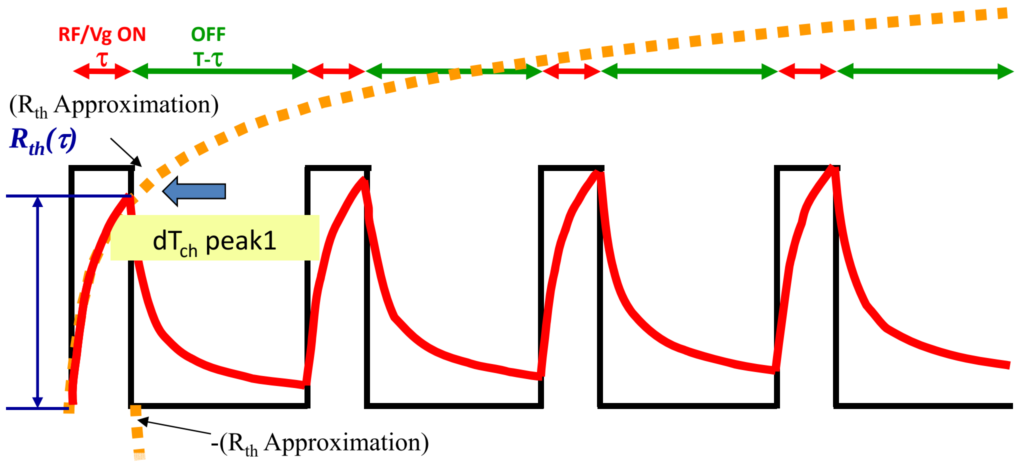
- **Designed for CW and saturated operation . (Most severe thermal requirement)**

Case.1 Rader (Pulsed operation)



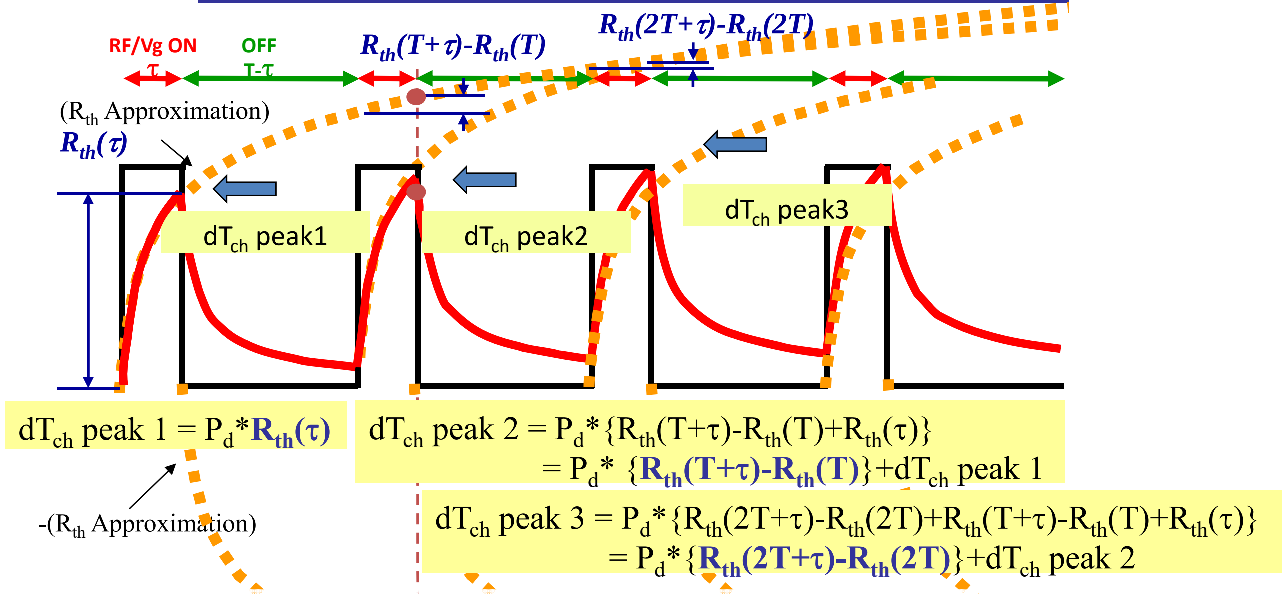
- Thermal design of pulsed operation chip differs from CW one, and the estimation of the transitional Tch is important. The following slides explain the detail.

Channel Temperature Simulation using Transient Thermal Resistance



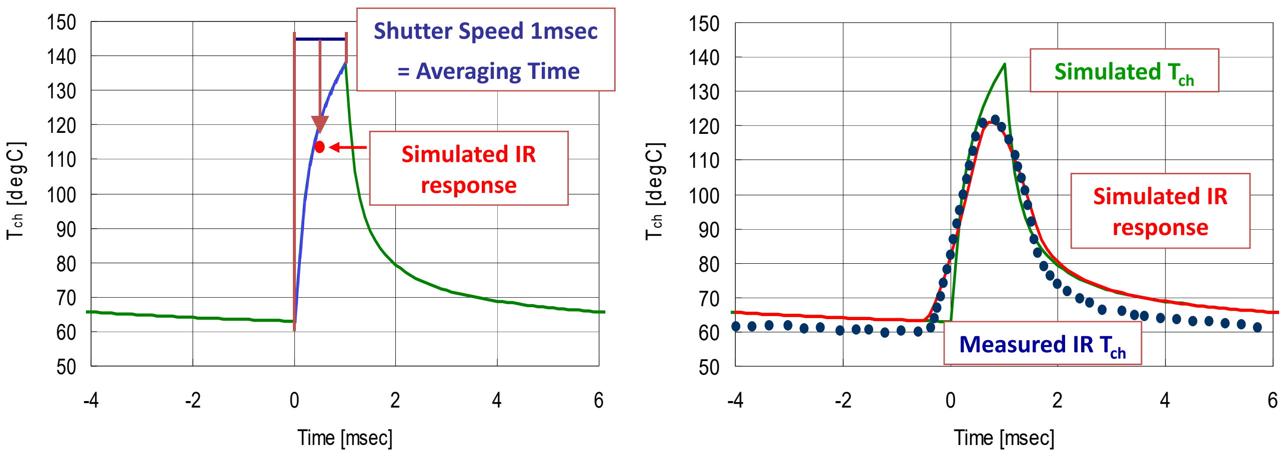
- During the pulse-ON, channel temperature rises due to the heat generation.
- At the pulse-OFF, the channel temperature falls down by heat dissipation, which is expressed as reverse behavior of heat generation.
- With combining these 2 lines, the channel temperature falls.

Channel Temperature Simulation using Transient Thermal Resistance



- The peak Tch at the 1st pulse is calculated as shown in above.
- The 2nd peak Tch is also calculated, combining these 3 values.
- The total Tch rise is summation of the delta Tch at the each on-state condition.

Channel Temperature Measurement & Analysis



- The analysis performed more than 10 years ago. We only had an IR system with rather slow shutter speed. But we found the measured Tch from IR agreed with the simulated Tch curve, by taking the shutter speed into consideration.
- Thus, we concluded that the mentioned simulation in previous slide is reliable. And the compact kW-class GaN device was developed by utilizing this analysis.

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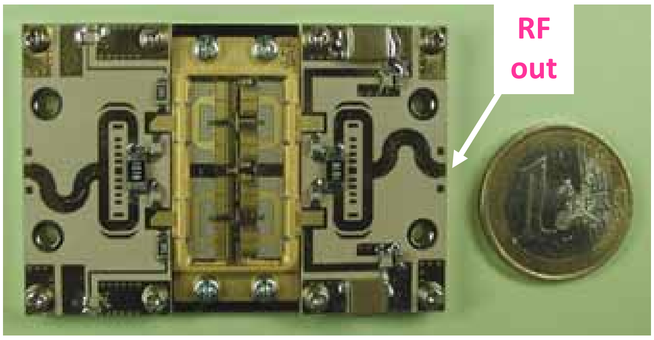
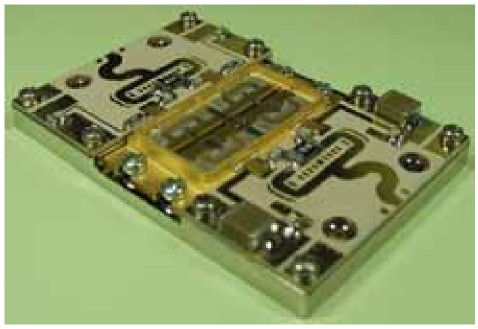
kW-Class GaN HEMT Pallet Amplifier for Radar

VGG VDD

RF in





VGG VDD

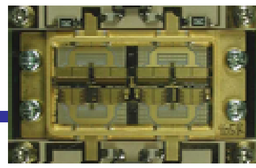
Size : 58.5 mm X 40.0 mm X 8.0 mm

- Input/Output matched to 50 ohm
- Includes RC Bias Circuit
- Cu base

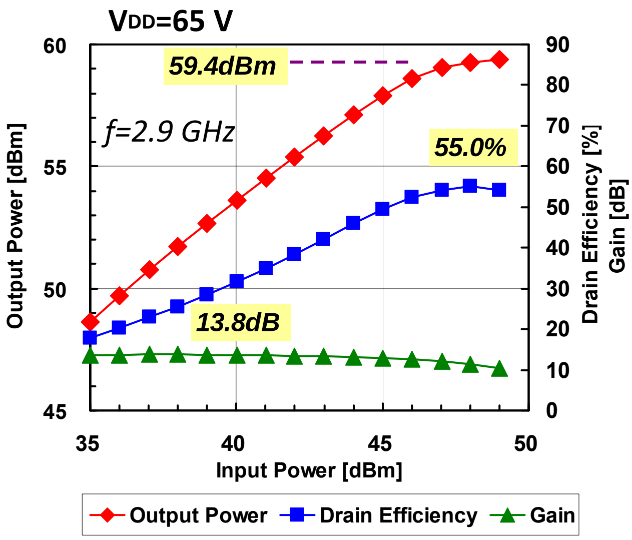
E.Mitani et.al, " A kW-class AlGaN/GaN HEMT pallet amplifier for S-band high power application ," EuMIC2007.

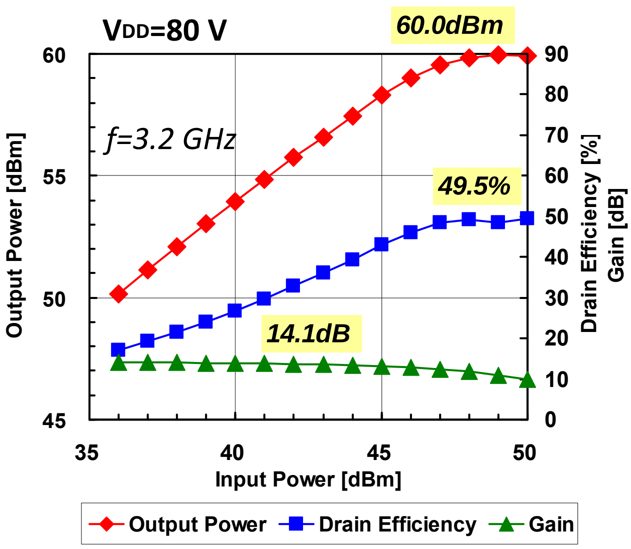
EuMW 2016
Microwaves Everywhere

kW-Class GaN for Radar RF Performance



I_{DD}(DC)=2.0A, Pulse Width 200μsec, Duty 10%



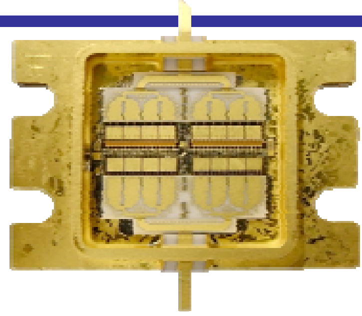


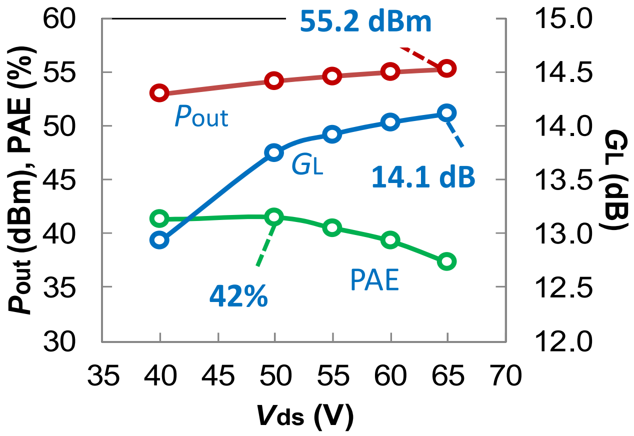
➢ Compact 1 kW class GaN HEMT for radar application has successfully demonstrated, by optimizing for pulsed operation.

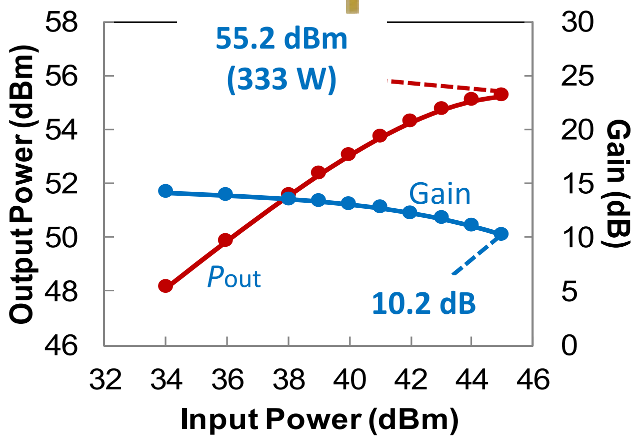
Up-to-date Achievement
X-band 300 W GaN HEMT for Rader

K.Kikuchi et.al, " An 8.5–10.0 GHz 310 W GaN HEMT for radar applications", 2014 IEEE MTT-S Int. Microwave Symposium Digest, 2014.

PKG size	**: 24.0 mm × 17.4 mm**
Gate width	**: 14.4 mm × 2chip (>10 watt/mm)**
Chip size	**: 5.4 mm ×0.7 mm**
Chip outline	**: Lg=0.4μm, Via-Hole**





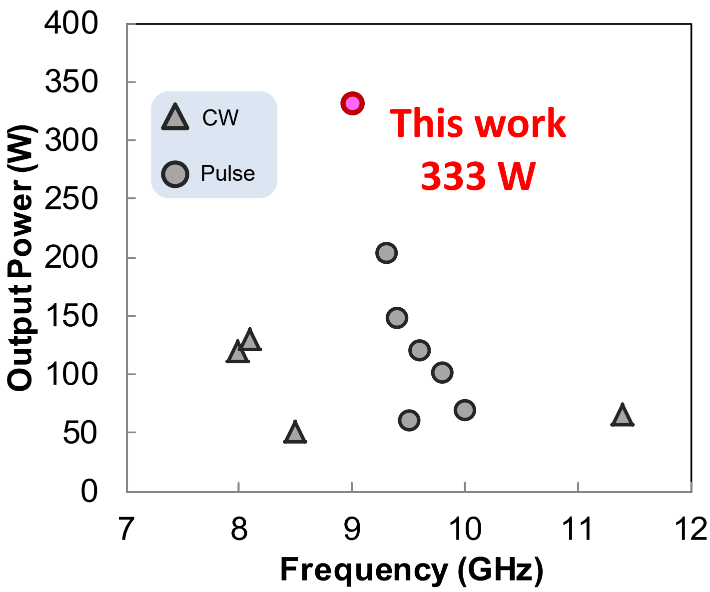


Pulse Width = 100 μsec, Duty = 10%, Frequency = 9.0 GHz

Up-to-date Achievement
X-band 300 W GaN HEMT for Radar

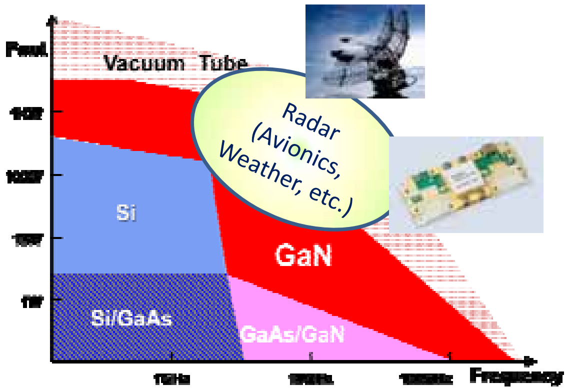
	This work (Maximum)
Frequency (GHz)	8.5 – 10.0 (9.0)
Output Power (W)	310 (333)
Power Gain (dB)	10.0 (10.2)

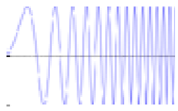
V_{ds} = 65 V, I_{dq} = 0.80 A
Pulse Width = 100 μsec, Duty = 10%



Prospect of Cost Effective GaN for Rader applications

- Using GaN to replace the klystron
  - High reliability, Maintenance free
  - Compact, Easy operation
  - -> <u>Reduction of OPEX</u>
- GaN output power is not as large as klystron, but it allows long pulses. Pulse compression can be used.
- Cost effective GaN HEMT will penetrate into the radar applications.

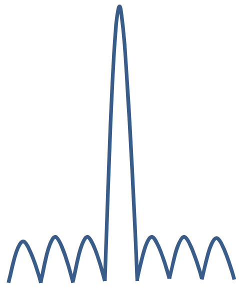




Linear FM Pulse

Filter

Frequency Dependent Delay Filter



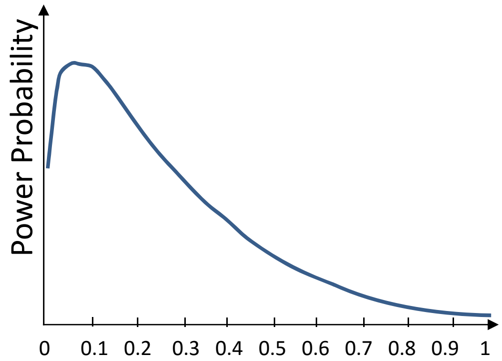
Compressed Pulse

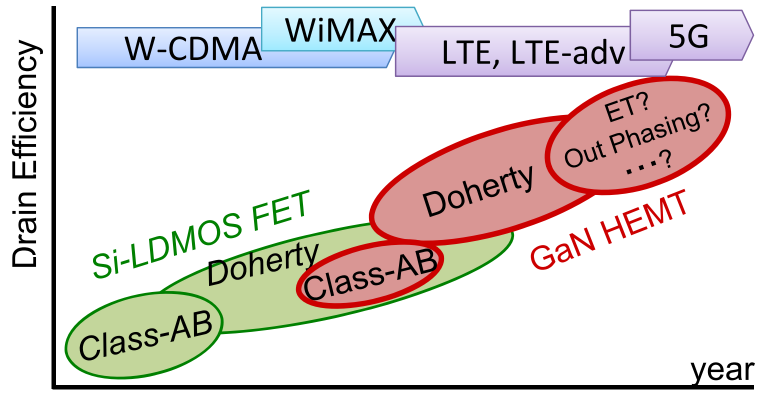
http://www.river.go.jp/xbandradar/

Outline

Case.2 BTS Application (Backed-off Operation)

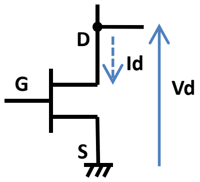
BTS trend → Smaller → Higher efficiency



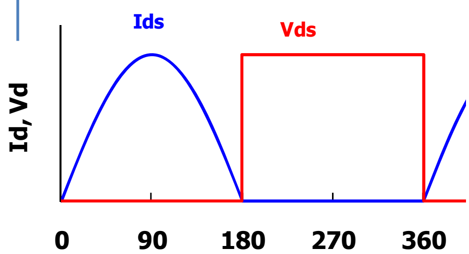


Both efficiency improvements of device itself & efficiency enhancement circuit techniques are required, at backed-off power region.

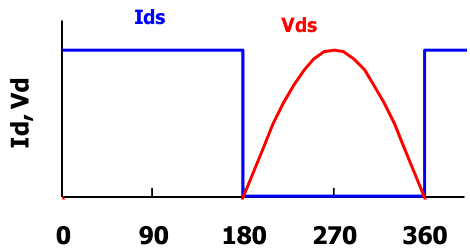
Operation Class (F, inverse-F)



Class-F



Inverse Class-F



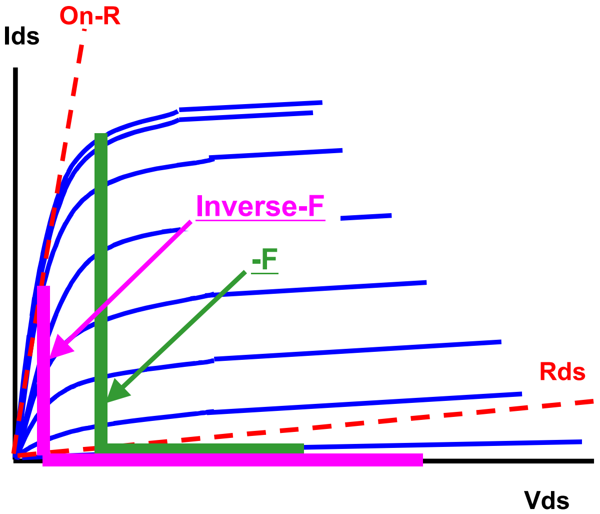
Load Impedance for Harmonics

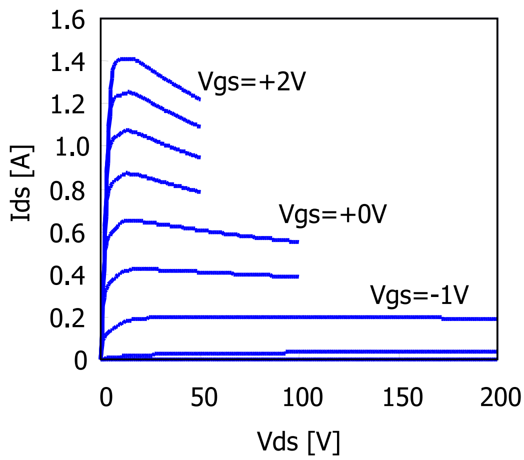
Class-F	Inverse Class-F
Even : 0 (Short)	Even : ∞ (Open)
Odd : ∞ (Open)	Odd : 0 (Short)

Peak Value of Voltage, Current

Class-F	Inverse Class-F
Voltage: 2x Vds(DC)	Voltage: 3.14x Vds(DC)
Current: 3.14x Average Ids	Current: 2x Average Ids

Combination of Inv. Class-F & GaN HEMT Property

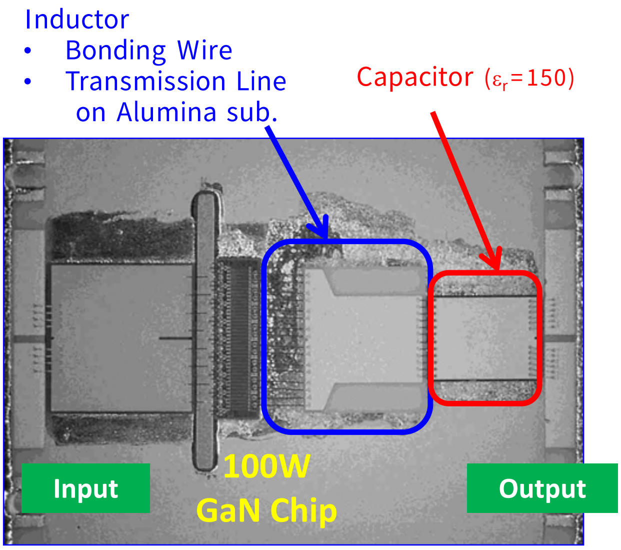


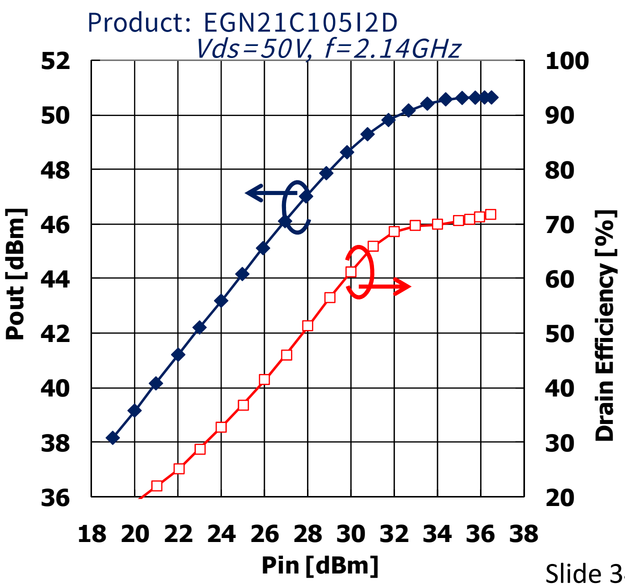


- Inverse Class-F requirement are,
  - Low Ron (Steep Knee) reduces RF-loss
  - High breakdown voltage contributes to keep good pinch off
- GaN HEMT is the best technology for these requirements at present.

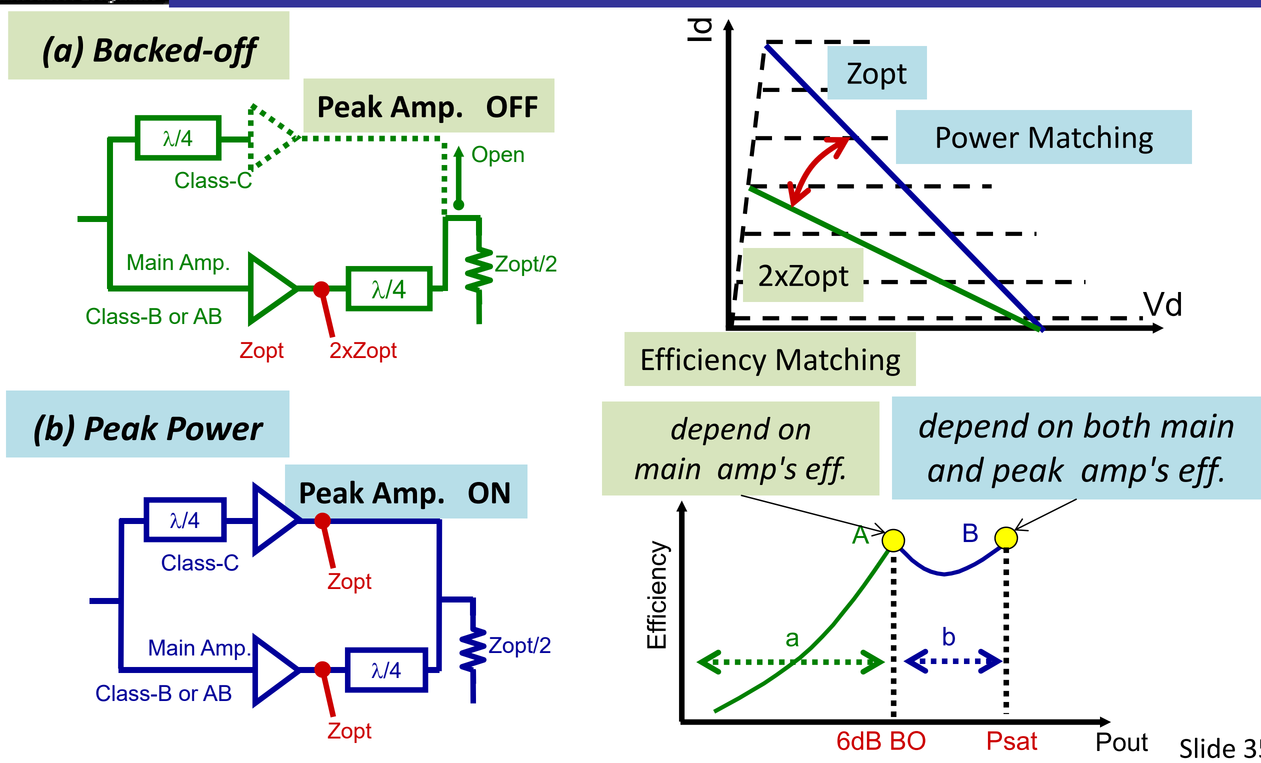
Circuit of Inverse Class-F 100W GaN HEMT

Design Concept
Circuit : Harmonic tune by simple(=low cost) LC circuit (LPF)
GaN chip : Size minimization by referring thermal loss

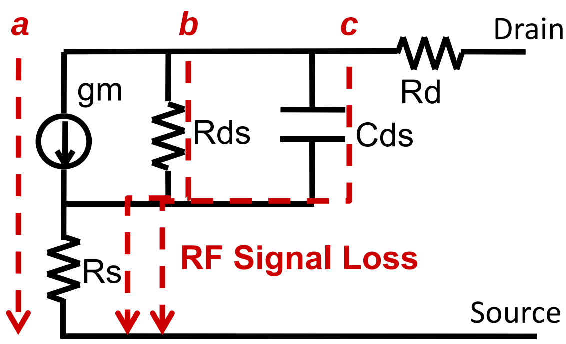


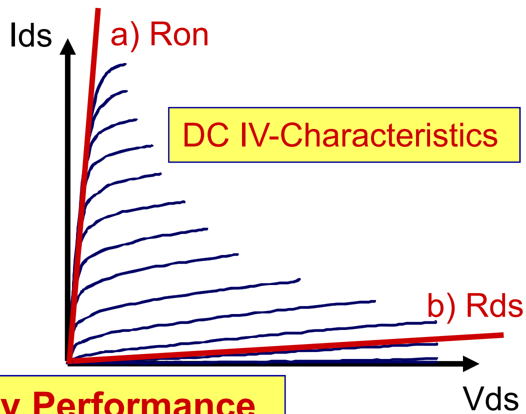


Theory of Doherty Amplifier



GaN HEMT for Doherty PA





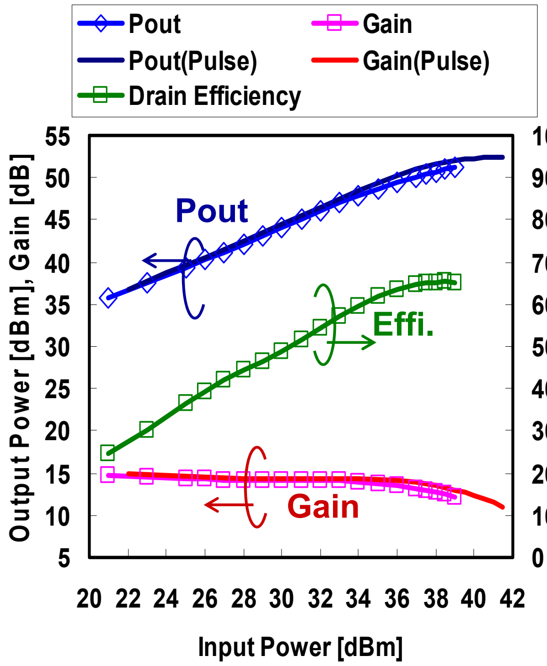
c) Cds Key of High Frequency Performance

70W-class Device for 2.6GHz Base Stations

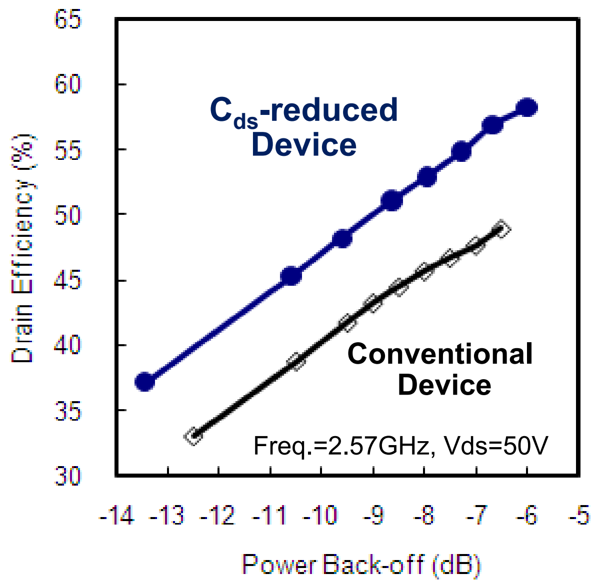
70W-class Device	Vds	Imax	Wg	Cds
Si LDMOS-FET	28V	26A	120mm	31pF
GaN HEMT (This work)	50V	11A	18mm	**3.8pF**

H. Deguchi et.al, "A 33W GaN HEMT Doherty Amplifier with 55% Drain Efficiency for 2.6GHz Base Stations", 2009 IEEE MTT-S Int. Microwave Symposium Digest, pp.1273-1276, 2009.

RF Performance of Doherty PA

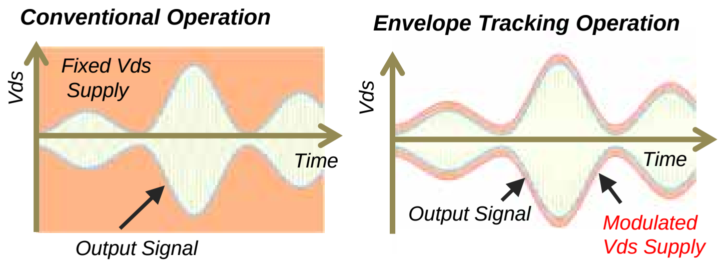


Vds = 50V, Idq-m = 200mA Idq-p : Class-C Bias
f = 2.6GHz, CW Pulse Duty = 10% (6μs/60μs)



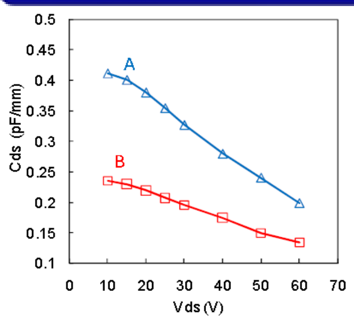
H. Deguchi et.al, "A 33W GaN HEMT Doherty Amplifier with 55% Drain Efficiency for 2.6GHz Base Stations", 2009 IEEE MTT-S Int. Microwave Symposium Digest, pp.1273-1276, 2009.

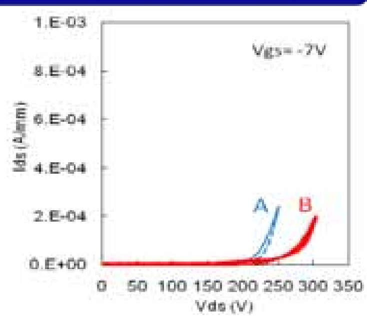
Example of Envelope Tracking (ET)



GaN HEMT for Envelope-Tracking

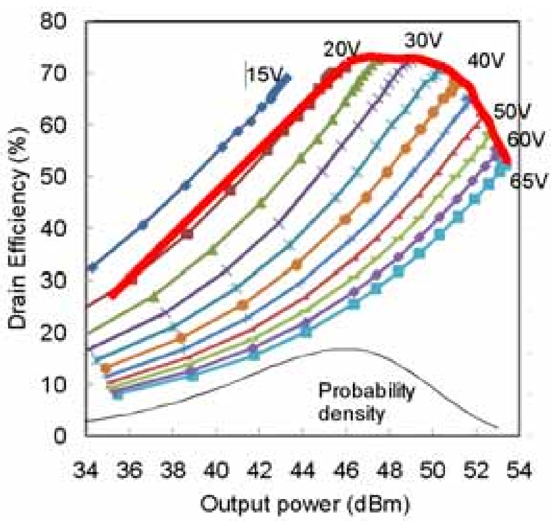
1. ***Cds reduction & Vds dependence reduction***
2. ***BVdsx ≧300 V , for 20-65V ET-operation***





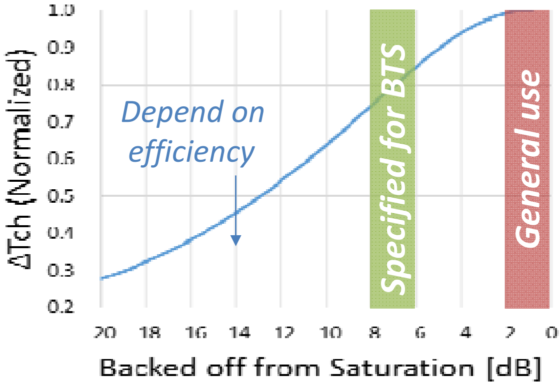
Imax =680mA/mm, Cds=0.15pF/mm, BVdsx≧300V

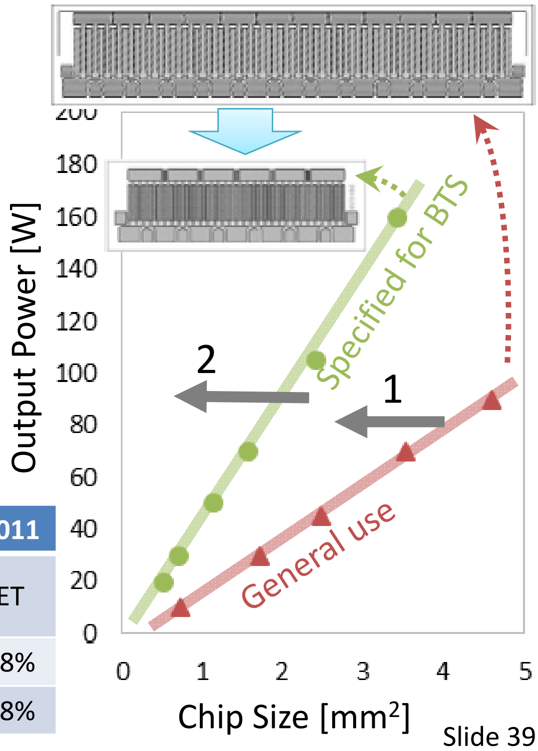
F.Yamaki et.al, " A 65 % drain efficiency GaN HEMT with 200 W peak power for 20 V to 65 V envelope tracking base station amplifier ," 2011 IEEE MTT-S Int. Microwave Symposium Digest, 2011.



Optimum Thermal Design for BTS

1. Thermal Design



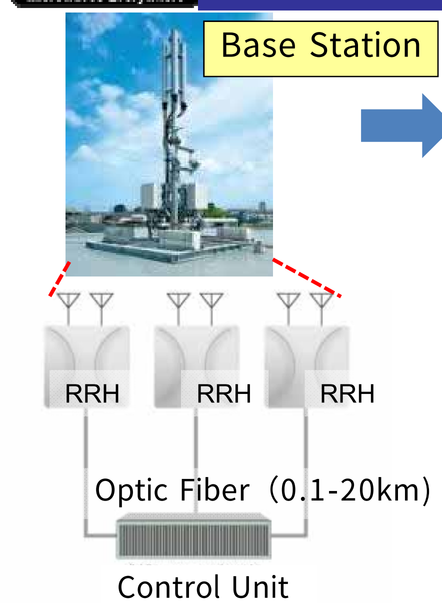


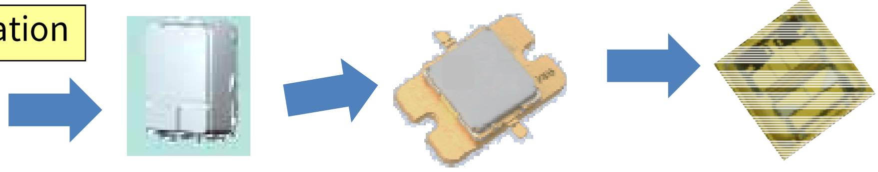
2. Efficiency Boosting

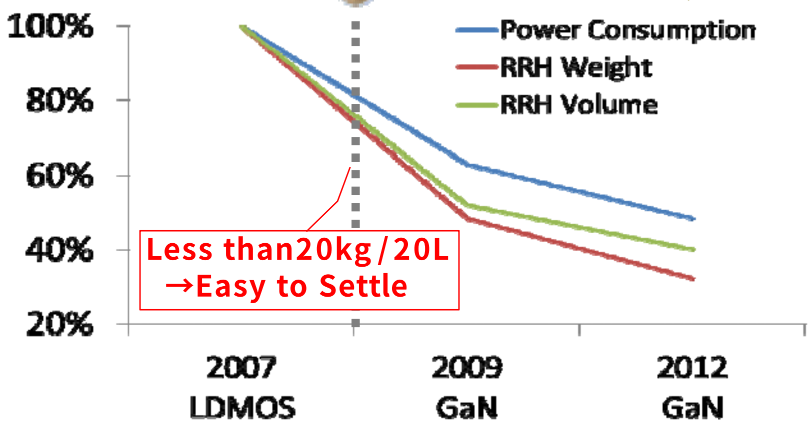
	～2005	2006	2009	2011
Circuit Technique	Class-AB	Higher Class	Doherty w/Class-F $^{-1}$	ET
Drain Eff. @8dB-B.O.	34%	45%	55%	68%
Thermal Dissipation	Ref.	83%	68%	48%

RRH* BTS-system and GaN HEMT

* Remote Radio Head



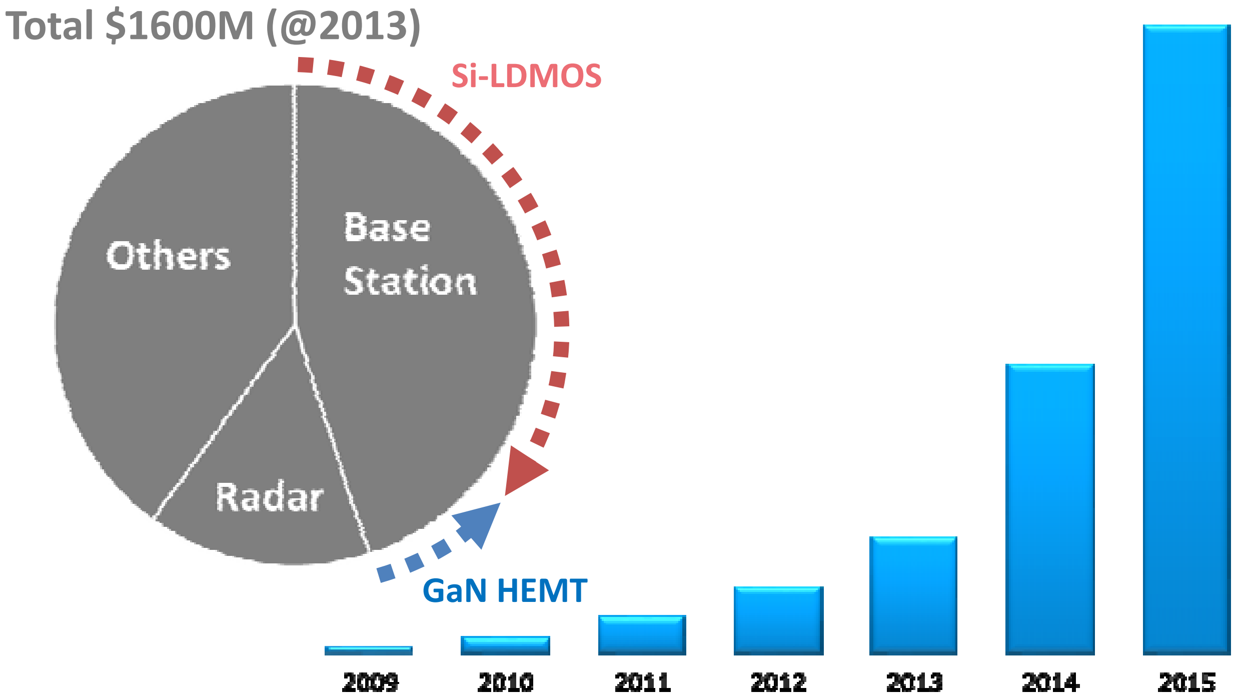




CAPEX (Capital Expenditure) -> Cost reduction of GaN itself has been progressed, and small & light weight PA, utilizing GaN high efficiency, contributes to BTS setting cost.

OPEX (Operating Expenditure) -> Higher efficiency PA realizes lower power consumption.

Microwave Device Market & SEI GaN HEMT Shipment



Outline

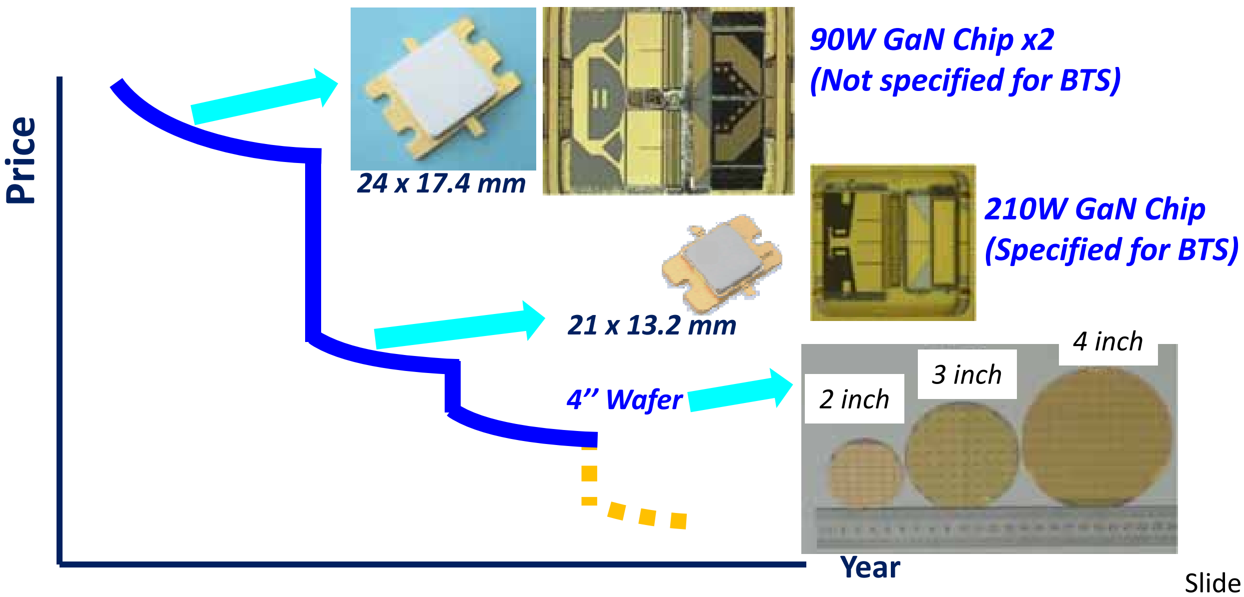
1. Fundamentals
2. Thermal Study of Substrate
3. Thermal Design (GaN for Radar)
4. Thermal Design (GaN for Base Station)
5. Summary

Summary (1/2)

- GaN HEMTs have already realized high quality, uniformity and reliability for infrastructure RF power applications. Thus, the cost reduction has been strongly required.
- The adequate thermal transfer design is one of the solutions. GaN on-SiC has been proved the best material to satisfy both the cost and thermal requirements. The focus design on pulsed operation is effective for compact radar devices, and the efficiency boosting in backed-off region have reduced the chip size of base station PAs.

Summary (2/2)

- GaN HEMT has already been adopted in several markets. For further market penetration, continuous cost down efforts are essential.



Cost effective approaches for European GaAs & GaN Power solutions

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Outlilne

What can be the reducing cost drivers for GaN on SiC solution ?

- Presentation of UMS
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution
- UMS Products & Foundry Solutions
- Conclusions

Outlilne

- Presentation of UMS
  - III-V company with 20 year experience in semiconductor (especially GaAs HEMT)
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution
- UMS Products & Foundry Solutions
- Conclusions

UMS at a glance

- Founded in 1996 by gathering Thales and AIRBUS Defense and Space GmbH activities
- European source of RF MMIC solutions, GaAs and GaN foundry services
- 2 industrial facilities in **Ulm** (Germany) & **Villebon** (France)
- 400 people

Villebon facility

Ulm facility

Outlilne

- Presentation of UMS
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution
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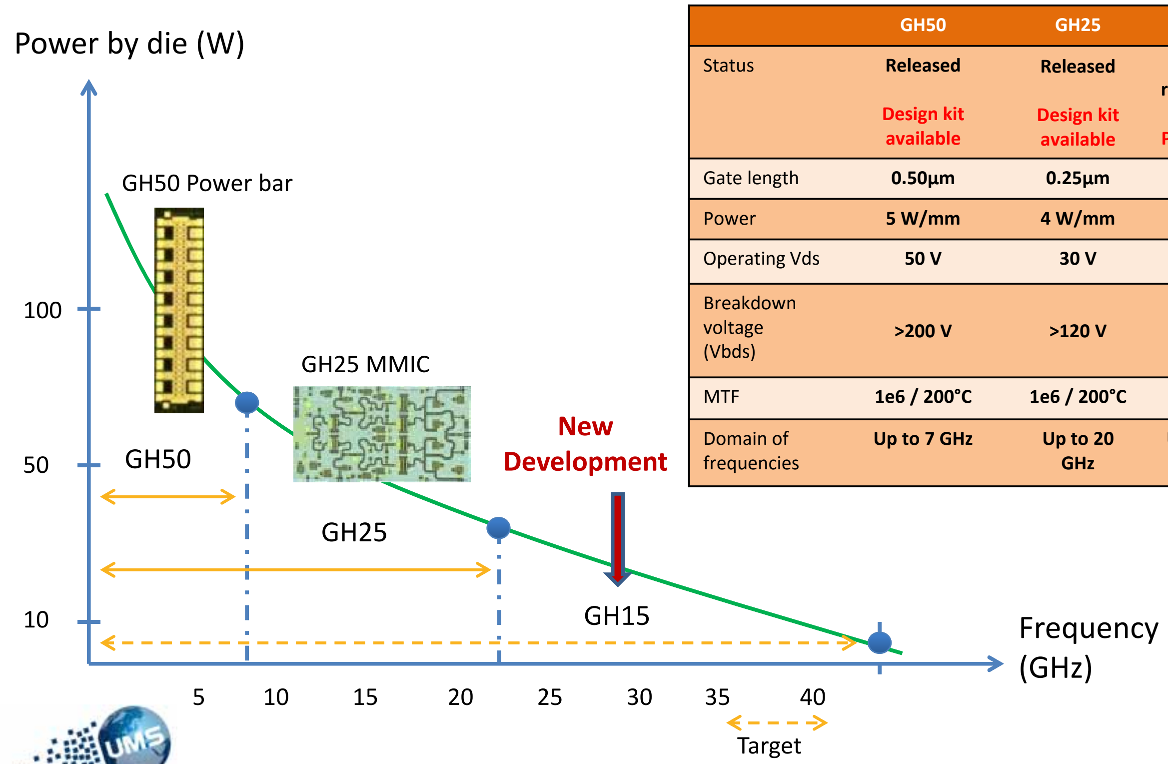
- Conclusions

UMS GaN technologies

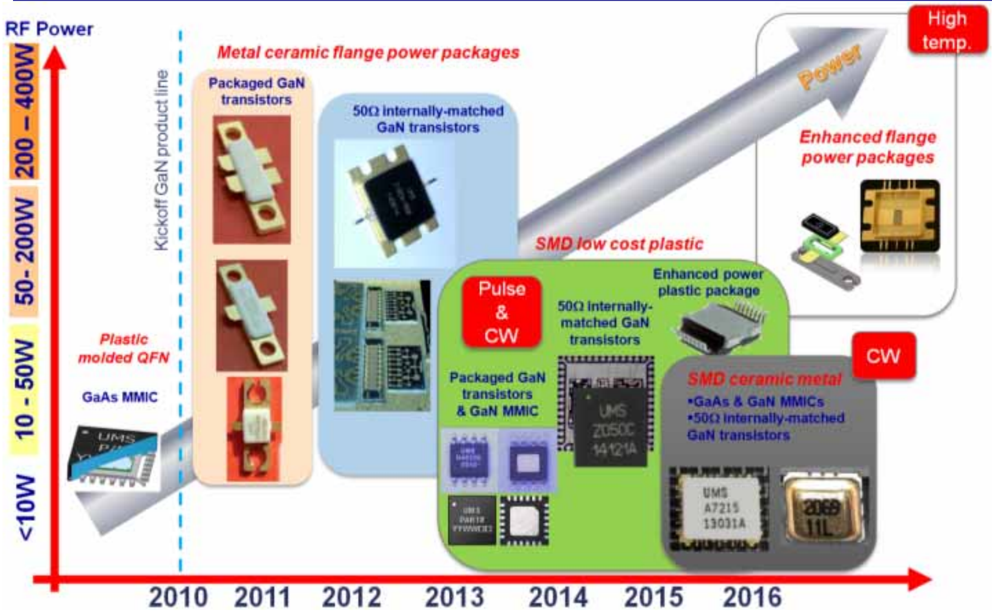


	GH50	GH25	GH15
Status	**Released** **Design kit available**	**Released** **Design kit available**	**To be released 2017** **Targeted Performances**
Gate length	**0.50µm**	**0.25µm**	**0.15µm**
Power	**5 W/mm**	**4 W/mm**	**3.5 W/mm**
Operating Vds	**50 V**	**30 V**	**20V**
Breakdown voltage (Vbds)	**>200 V**	**>120 V**	
MTF	**1e6 / 200°C**	**1e6 / 200°C**	**1e6 / 200°C**
Domain of frequencies	**Up to 7 GHz**	**Up to 20 GHz**	**Up to 40GHz**

Outlilne

- Presentation of UMS
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution
  - Various Packaging solutions
  - Thermal management of QFN
    - oPCB / Glue / Die Coating
- UMS Products & Foundry Solutions
- Conclusions

Packaging offer for power



Main constraints for GaN packaging - related to costs:
- Frequency band
- Thermal management

Thermal management analysis

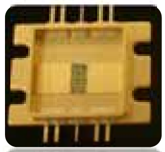
Different solutions investigated:

- Package solutions:
  - Flange
  - Ceramic metal SMD
  - SMD QFN
- Stack variation
  - PCB variations
  - Interlayer stack
    - Mo / Diamond Tab
    - CuMo Coin

Plastic molded QFN

Ceramic metal SMD

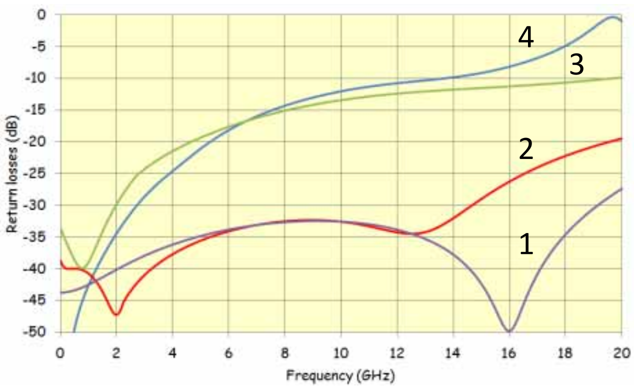
Flange package



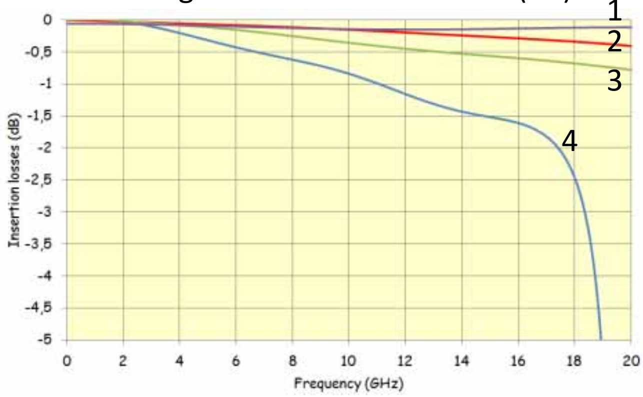
Broad band packages

1: Plastic molded QFN
2: Enhanced flange package
3: Ceramic metal SMD
4: Flange package

Package + PCB return losses (dB)



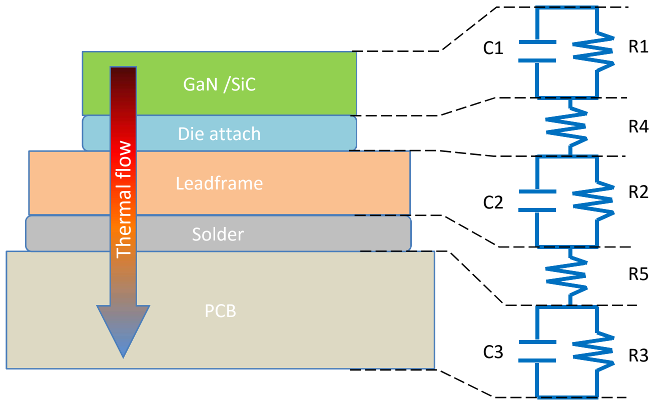
Package + PCB insertion losses (dB)



- SMD QFN package is excellent
- Flange packages are competitive up to 20GHz
  - Package optimization still ongoing to achieve VSWR <1.5:1 at 20GHz
  - Part of the matching can be integrated into the die

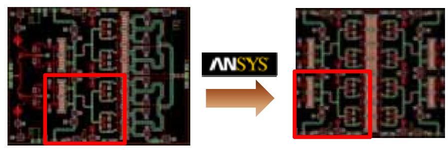
Package Thermal analysis

Target: Package GH50 & GH25 products



- Analysis must be carried out on different samples:
  - Power-bares
  - MMICs
- Finite element simulations performed on different 3 mains package family – ANSYS

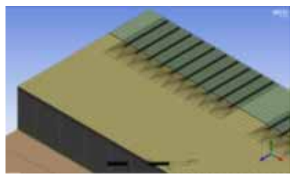
MMIC Packaging: Modeling assumption

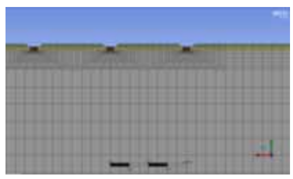


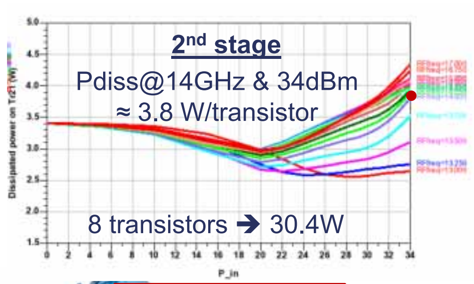
Test Vehicle GH25 MMIC:
1^{st} stage : 4x8x125µm
2^{nd} stage : 8x8x150µm

Analysis performed on ANSYS:

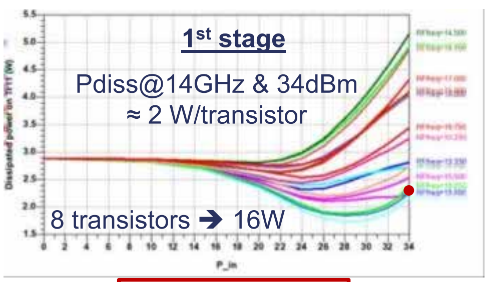
- Symmetry : ¼ of the device is meshed
- GaN/SiC interface ➔ Layer with low thermal conductivity (TBR)
- Joule heating ➔ Block heater along drain edge of gate foot (≈ 1.5 µm)
- Boundary condition ➔ Fixed temperature on backside of full assembly
- Meshing ➔ Specific methodology for power bars ≈ 1 000 000 nodes







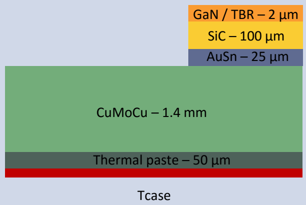
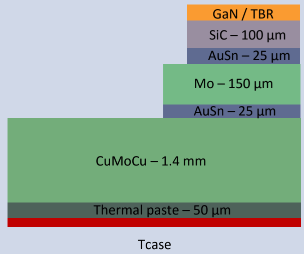
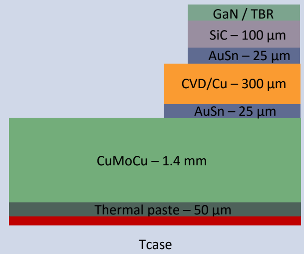
P_{diss} = 3.16W/mm



P_{diss} = 2W/mm

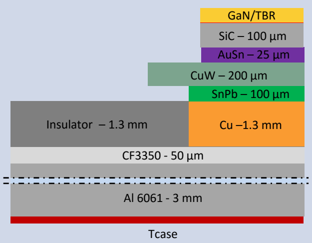
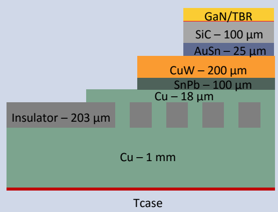
Flange Package

Tc = 80°C / Pdiss : 2nd stage ➔ 3.16 W/mm (30.4 W) / 1st stage ➔ 2 W/mm (16 W)

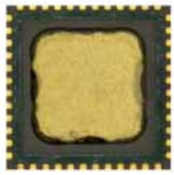
Cases	Flange KYO	Flange KYO + Tab Mo	Flange + Tab Diamond
Stack			
Rth_tot (°C/W)	3.75	3.84	3.24
Tj _max (°C)	194	196.8	178

Ceramic metal SMD

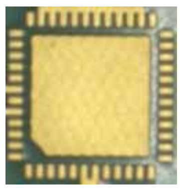
Tc = 80°C / Pdiss : 2nd stage ➔ 3.16 W/mm (30.4 W) / 1st stage ➔ 2 W/mm (16 W)

Cases	SMD & PCB coin	SMD & PCB vias
Stack		
Rth_tot (°C/W)	5.06	4.69
Tj _max (°C)	233.8	222.7

PCB Coin Footprint

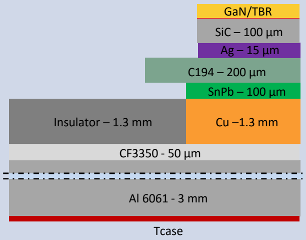
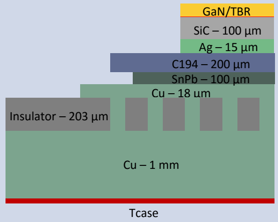


PCB Via Footprint



Plastic Package SMD QFN

Tc = 80°C / Pdiss : 2nd stage ➔ 3.16 W/mm (30.4 W) / 1st stage ➔ 2 W/mm (16 W)

Cases	SMD & PCB coin		SMD & PCB vias	
Stack				
Rth_tot (°C/W)	4.97[a]	4.72[b]	4.56[a]	4.32[b]
Tj _max (°C)	231[a]	224[b]	219[a]	211[b]

2 different Ag based glues evaluated:

a) 20 $W.m^{-1}.K^{-1}$
b) 70 $W.m^{-1}.K^{-1}$

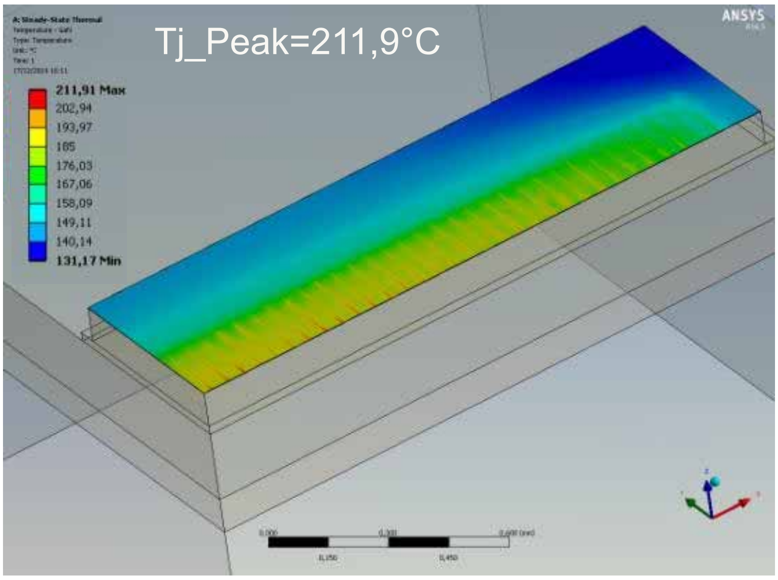
Synthesis

Case study	Packaging	Remark	Rth (°C/W)	Bandwidth	Cost
1	Flange KYO	Hermetic	3.75	Up to 6 GHz	☹
2	Flange KYO + Mo TAB	Hermetic	3.84	Up to 6 GHz	☹
3	Flange KYO + Diamond TAB	Hermetic	3.25	Up to 6 GHz	☹
4	SMD + PCB coin	Hermetic	5.06	Up to 14 GHz	😐
5	SMD + PCB via	Hermetic	4.69	Up to 14 GHz	😐
6	SMD QFN + PCB coin	Die attach : 20 $W.m^{-1}.K^{-1}$	4.97	> 20 GHz	☺
		Die attach : 70 $W.m^{-1}.K^{-1}$	4.72	> 20 GHz	☺☺
7	SMD QFN + PCB via	Die attach : 20 $W.m^{-1}.K^{-1}$	4.56	> 20 GHz	☺
		Die attach : 70 $W.m^{-1}.K^{-1}$	4.32	> 20 GHz	☺☺

Approach power bar assembly

Temperature Gradient

- 8x8x400µm / Tref = 75°C / P = 2W/mm/ CW



Die Attach Impact

- 8x8x400 / 7x7 QFN, CW, P=2W/mm, Tcase=75°C, Cond glue = 40W/m.K

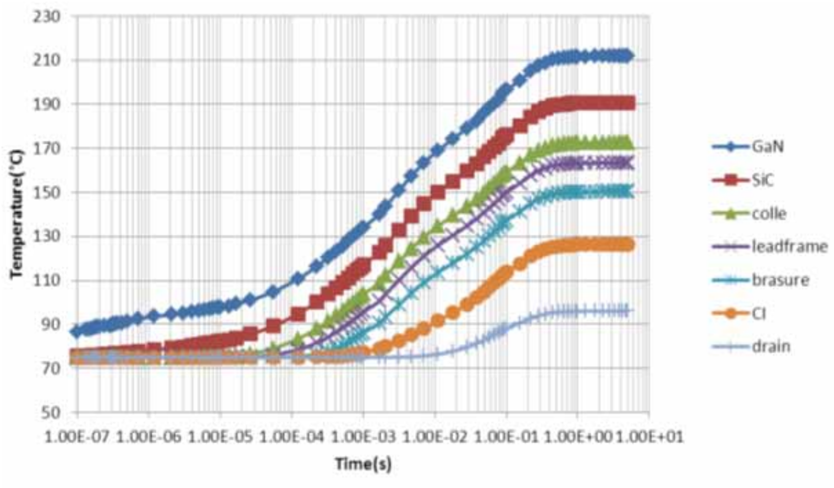
	T(°C)	delta T (°C)	Rth(°C/W)	contribution (%)
GaN / TBR	**217.9**	21.4	0.418	15.0
substrat SiC	196.5	18.2	0.355	12.7
colle puce (40W/mK)	178.3	15.6	0.304	10.9
Leadframe	162.7	12.7	0.248	8.9
BrasureSnPb	150.0	23.7	0.463	16.6
Cl/glue	126.3	30.3	0.591	21.2
Drain Al	96.1	21.1	0.411	14.7
Total	75	**142.9**	**2.792**	100.0

- 8x8x400 / 7x7 QFN, CW, P=2W/mm, Tcase=75°C, Cond glue = 20W/m.K

	T(°C)	delta T (°C)	Rth(°C/W)	contribution (%)
GaN / TBR	**230.9**	22.0	0.430	14.1
substrat SiC	208.9	18.4	0.360	11.8
colle puce (20W/mK)	190.5	28.9	0.565	18.6
Leadframe	161.6	12.1	0.235	7.7
BrasureSnPb	149.5	23.3	0.455	14.9
Cl/glue	126.2	30.1	0.588	19.3
Drain Al	96.1	21.1	0.411	13.5
Total	75	**155.9**	**3.046**	100.0

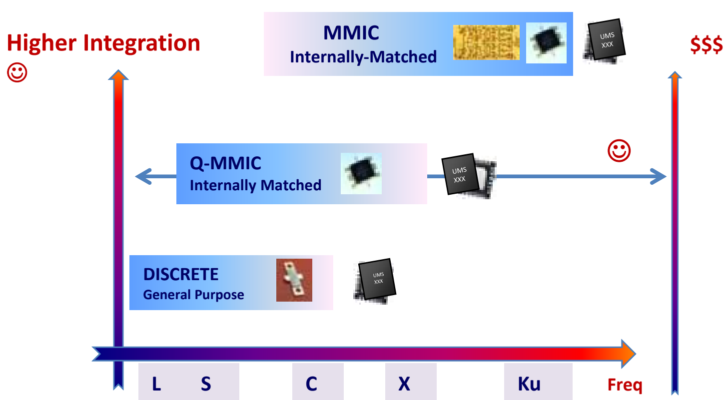
GH50 Power Bar / Transient

- 8x8x400 / 7x7 QFN / Tref = 75°C / P = 2W/mm



Conclusion on assembly

- SMD QFN solutions are broadband and lower cost solution
  - ➔ Applied to GH25 and GH50
- Analysis shows that thermal management strongly depends on the PCB
  - Coin offers very good thermal dissipation / difficult to implement to series
  - Thermal glue can reduce by roughly 0.2 $W.m^{-1}.K^{-1}$
- As demonstrated GaN on SiC packaged in QFN can also operate in CW
  - Important care must be take to the functioning conditions



Outlilne

- Presentation of UMS
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution
- UMS Products & Foundry Solutions
  - Foundry Presentation
    - o Market addressed are not only military
    - o Foundry partner contribution
  - Quasi-MMIC solution development
    - o Concept: Combination of GaN & GaAs
    - o Cost reduce
    - o Solutions
- Conclusions

UMS Foundry Solutions

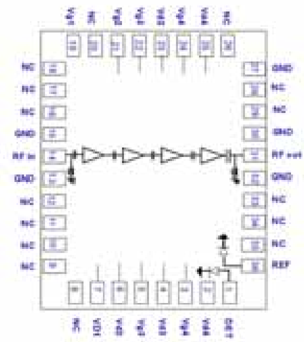
1W High Power Amplifier 37- 40GHz

PPH15X-20

Power detector inside, Gain Control

EuMW 2016 Microwaves Everywhere

Advanced concept / PPH15X-20 / QFN / CHA6194-QXG



- Application
  - *Point to point*
  - *Point to Multipoint*

- High linearity HPA
  - RF bandwidth: 37-40GHz
  - Linear Gain: 20dB
  - Power at 1dB comp.: 30dBm
  - Sat. Power : 31dBm
  - RL>13dB
  - Consumption: 6V, 0.8 A

- Specific features:
  - GaAs pHEMT process
  - Power detector dynamic 30dB
  - Low AM/AM, AMP/PM,
  - QFN 5x6

1W High Power Amplifier 37- 40GHz

PPH15X-20

Power detector inside, Gain Control

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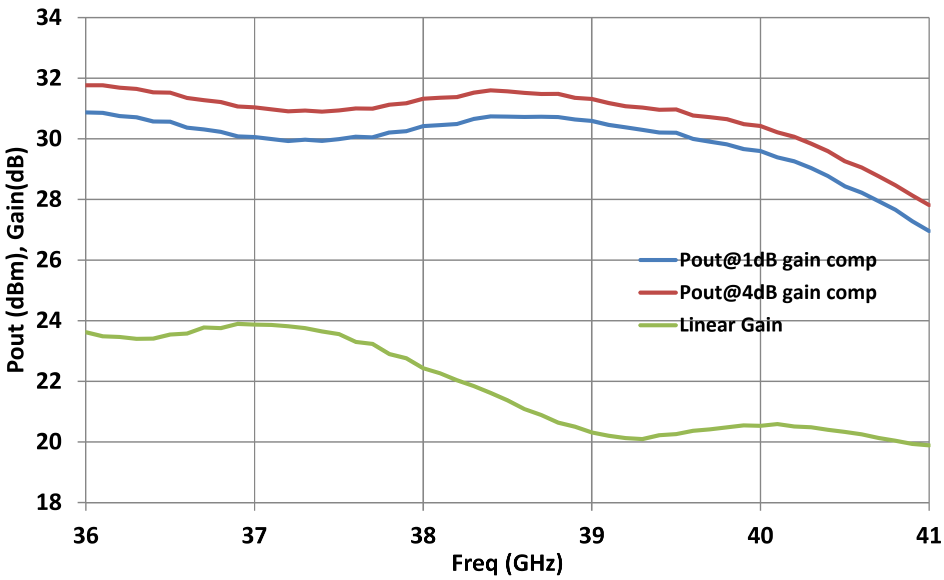
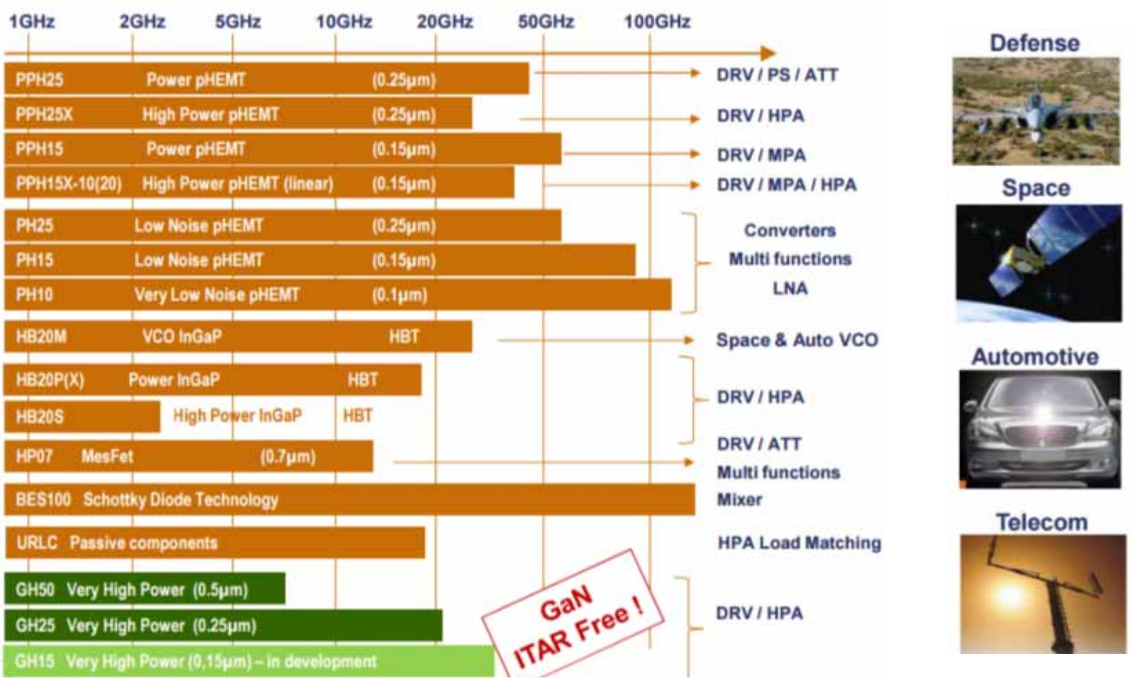
Vd=6V Idq=0.8A

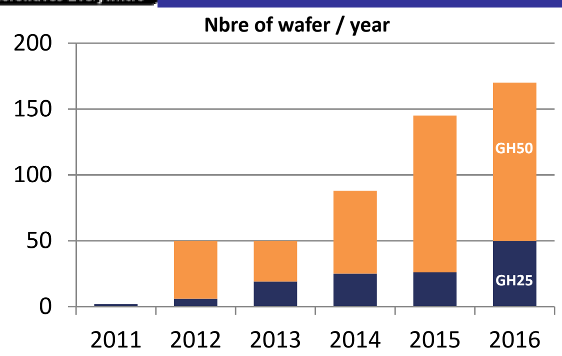


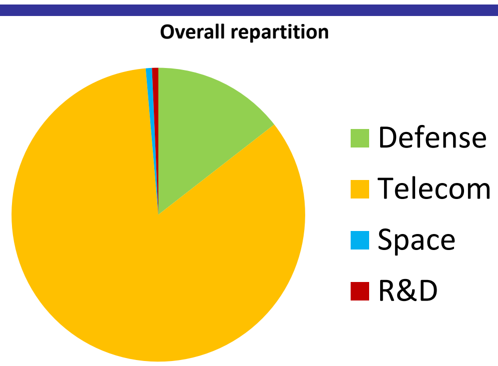
Foundry Portfolio



➢ QFN Assembly offer for all processes

GH50 & GH25 Foundry key figures





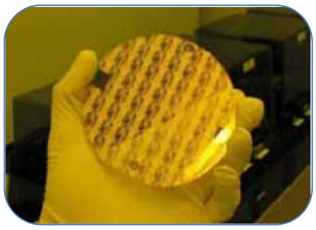
- GH25: Since 2010 more than 130 wafers processed in the frame of 80 different projects
- GH50: Production launched and transferred to 4''
- More 150 wafers to be manufactured in both GH50 & GH25 in 2016
- Design Kit including EM Stack and DRC for ADS2016

DK available for GH25-10

- **GH25: MMIC process: Qualified & Open in Foundry**
  - 250nm gate length
  - On 4-inch SiC wafer
  - Frequency range: DC – 20 GHz
  - V_{ds} = 30V as standard Recommended Operating Value
  - I_{dss} = 850 mA/mm as average value
  - Very High breakdown voltage: V_{bds} > 120V
  - Power density: 4W/mm @ 10GHz in CW Mode
  - Design Kit available for ADS2009-2016 & MWO
    - NL model for Hot FET (electrothermal)
    - L FET model for noise
    - NL model for Cold-FET
    - NL model for diodes

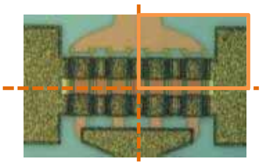
(Scalable models for passives and active elements)

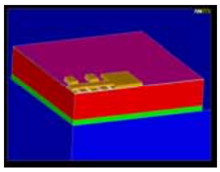
  - New features: DRC & Stack EM available for ADS2016

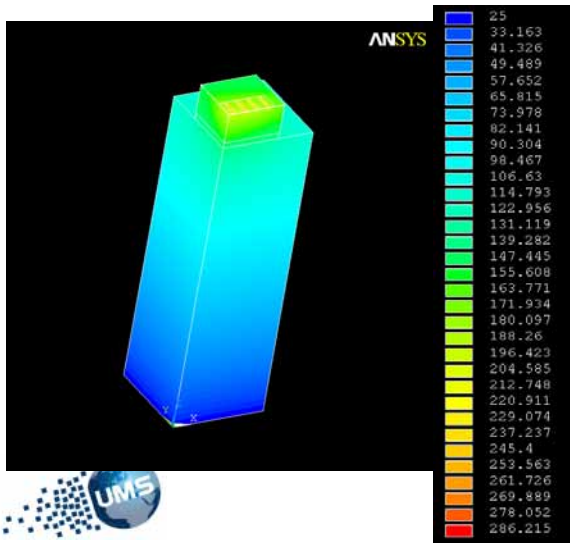


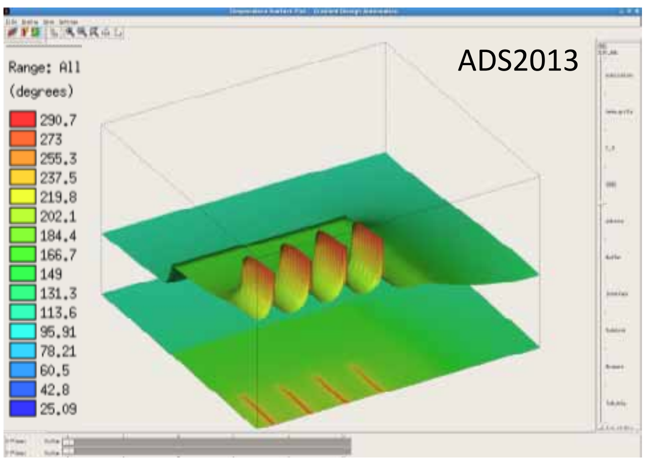
ANSYS/ADS Thermal analysis

- Transistor GH25 8x125 d'UMS / V_{ds}=25V I_{ds}=25mA/mm







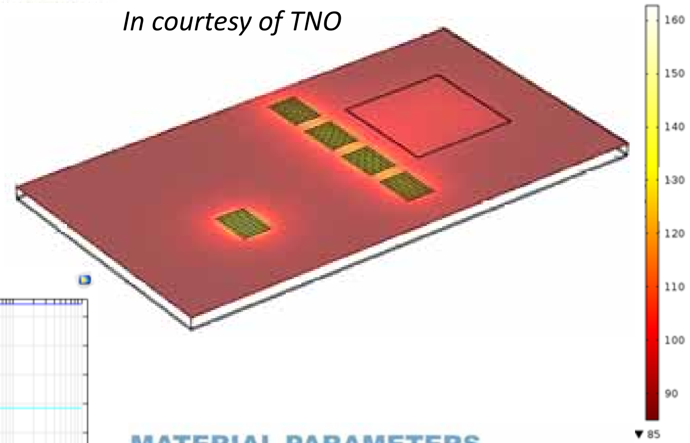


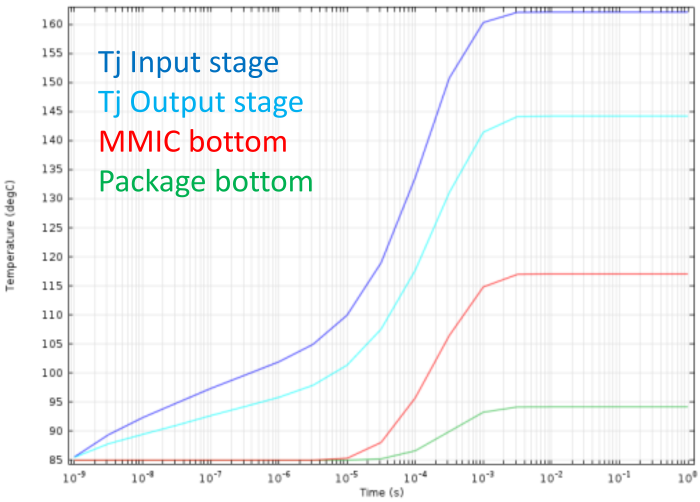
TNO – HPA GH25-10 design

In courtesy of TNO

THERMAL SIMULATION

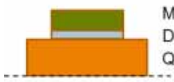
- Input stage 1x10x275um, Pdiss=8.2 W
- Output stage 4x10x275, Pdiss=23.3 W
- Matching networks, Pdiss=7.2W
  (= Pdiss_total - (input+output stage))





MATERIAL PARAMETERS

	Thermal Conductivity	Heat Capacity	Density
	K (W/m.K)	C (J/kg*K)	Rho (kg/m^3)
SiC (worst case)	330 (T/300)^ -1.5	690	3216
Gold	317	129	19300
Ablebond-2815A	20	235 ? (Silver)	4900 ? (~50% Silver)
Copper QFN	380	385	8700



MMIC 100 um
Die-attach 20 um
QFN (copper) 200 um

Simplification of QFN package

Ta=85°C

UMS product Solutions

CHK015A-QBA

Product

DC - 6 GHz Packaged Transistor

- Application
  - *Radar & Communications*

General Purpose Transistor

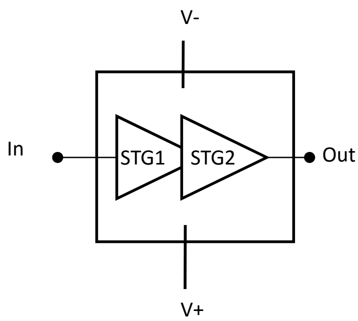
- RF bandwidth: DC – 6GHz
- Linear Gain: 14dB @ 6GHz
- Output Power: > 15W
- Drain Efficiency: > 70%
- PAE: 50% @ 6GHz
- Package: DFN 3x4

- Specific feature
  - Wide-band
  - Low parasitic Plastic Package
  - Low thermal resistance

25W / X-band / QFN

Sampling Now

In sampling / GH25 Based / Die product to be packaged



- Application
  - *Defence / Space*

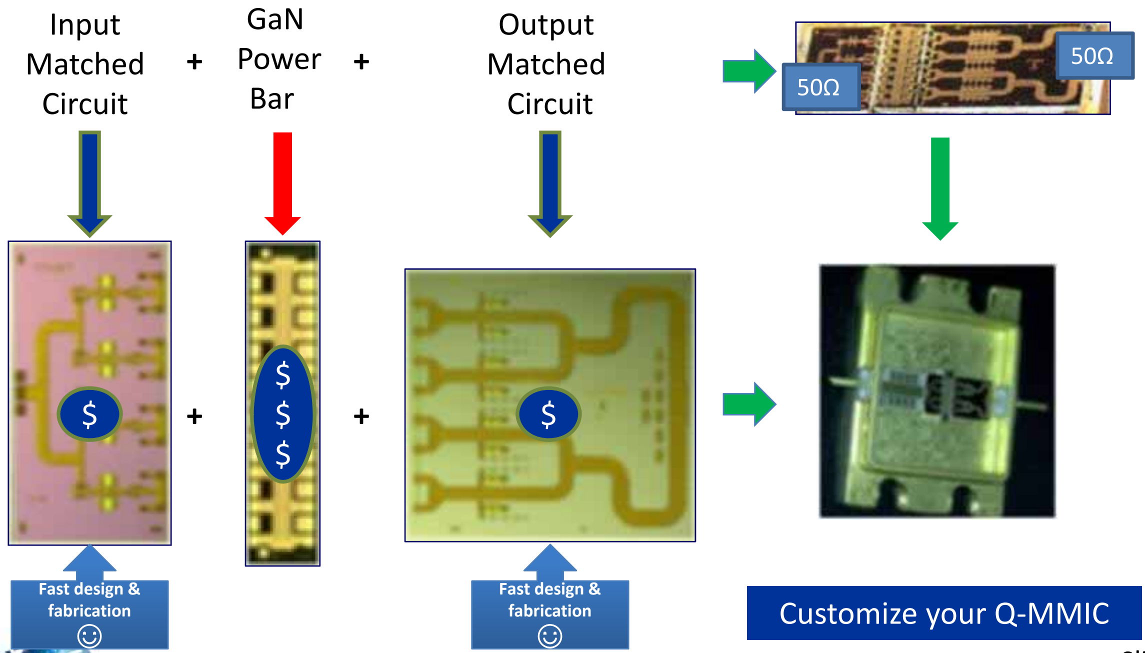
Main Performances

- RF bandwidth: 8.5 – 10.5GHz
- Gain: 30dB
- Pout : 25W
- PAE_associated: 45%
- Consumption: 30V, 0.8A

- Specific feature
  - High efficiency
  - High power
  - Die / 15W version available in QFN

Quasi MMIC Concept

Use of UMS proprietary Passive MMIC Technology: **Q-MMIC is close to MMIC size**

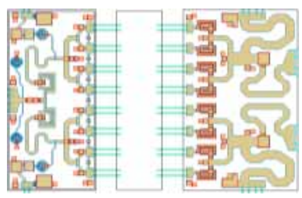


Customize your Q-MMIC

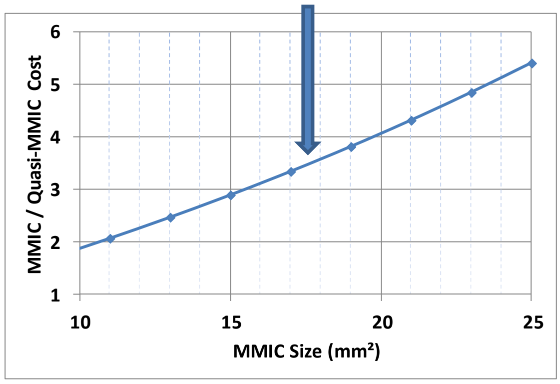
Why "Quasi MMIC"?

- **Integration**
  - Close to MMIC size
- **Cost**
  - Close to hybrid solutions
- **Flexibility**
  - Short dev. cycle times (passive MMICs)
    - GH50/25: 14Weeks ICT
    - URLC: 5 Weeks

Example of 50W C-band HPA



6mm² 3.6mm² 7.6mm²

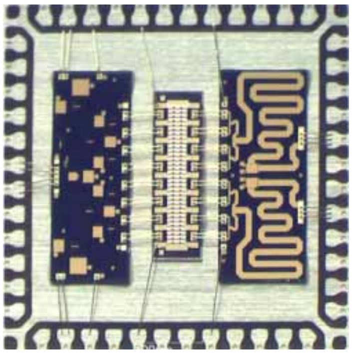


Applicable to QFN for low cost development

100W / L-band / QFN

New Product

In development / GH50 based / Internally-Matched / Q-MMIC



- Application
  - *Radar / Dual Use*

Main Performances

RF bandwidth:	1.2 – 1.4GHz
Linear Gain:	15dB
Output Power:	100W
Gain @ 50W	10dB
PAE :	55%
Package:	DFN 7x7

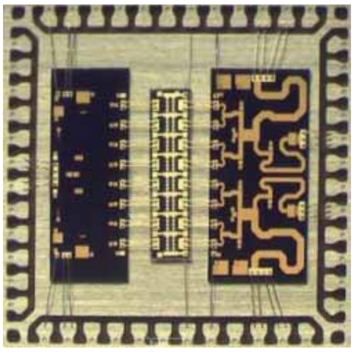
- Specific feature @ 1.3GHz
  - Peak Pout=110W
  - With PAE=57%
  - Gain = 14dB

"High Performance Plastic Packaged 100W L-Band Quasi-MMIC HPA" D. Bouw et al. - EuMC06-05

50W / C-band / QFN

New Product

In development / GH25 based / Internally-Matched / Q-MMIC



- Application
  - *Radar & Communications*

Main Performances

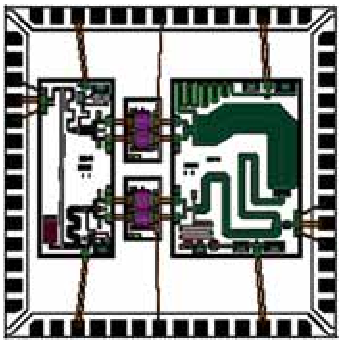
RF bandwidth:	5.2 – 5.9GHz	5.9-6.9GHz
Linear Gain:	14dB	13dB
Output Power:	50W	50W
Gain @ 50W	10dB	9dB
PAE :	47%	45%
Package:	DFN 7x7	DFN 7x7

- Specific feature
  - High PAE
  - Low parasitic Power Plastic Package
  - Low thermal resistance

C-band DPA Description

Advanced Development

Symmetric DPA Architecture / GH25 based / Q-MMIC / QFN packaging



- Application
  - *Communications / 5G*

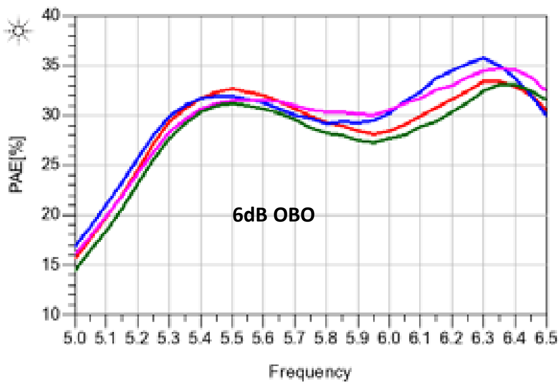
Main Objectives

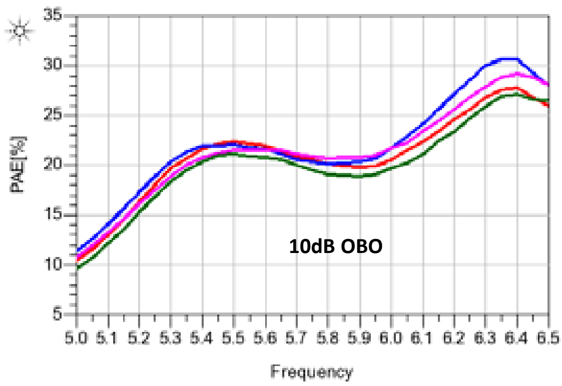
- **Configuration**
  - 1 stage => for investigations purpose
    - Single & dual input
    - Linearity / Main & Peak synchronization …
- **Key Performance**
  - Frequency band : 5.6 – 6.6GHz
  - Peak Output Power: 15W
  - PAE @ 6dB OBO: > 35%

C-band DPA Characterizations

PAE vs Freq / 6 & 10dB OBO / 4 Boards / T=25°C

- Biasing conditions:
  - Vd = 30V
  - Id_q_main = 60mA / Vgs0_peak = -7V





Outline

- Presentation of UMS
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution
- UMS Products & Foundry Solutions
- Conclusions

Conclusions

- QFN Solution validated for power technologies up to 40GHz – including GaN
  - MMIC in QFN for GH25 validated with enhanced glue + PCB solutions
    - High efficiency solutions already available
  - Q-MMIC in QFN used for GH50 & GH25
    - Challenging solutions evaluated
  - Release of PPH15X-20 for applications up to 40GHz
- Foundry access allowing more and more QFN assembly
  - Tools available for ADS allow more accurate thermal analysis
  - Association with URLC (passive process) available in Foundry
  - Indicators allow to identify the cost decrease (Industrial Manufacturing cycle time reducing, …)
- Final passivation is under development and should be available to improve the robustness versus humidity for GH50/GH25/URLC

Aknowledgment

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