Thermal Modeling and Characterization of a Gallium Arsenide Power Amplifier MMIC

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ABSTRACT

Thermal characterization of high power microwave devices is important for determining their reliability. Exceeding the optimal temperature will have a detrimental effect on the performance and reliability of these devices. However, temperature characterization of submicron features is often challenging and numerical simulations are often used. In this paper, a detailed finite element thermal model of a power amplifier Monolithic Microwave Integrated Circuit (MMIC) was developed and analyzed to obtain the peak operating junction temperature. Although detailed models would give more accurate results, they usually require more computational effort and time. Hence, a simplified finite element thermal model was also developed and its results compared with those for the detailed model. It was found that the results from the simplified model are higher than those from the detailed model by about 2°C/W to 5°C/W. The temperature distributions of actual MMIC devices were measured using IR thermography and thermoreflectance thermography. It was found that the temperature measured using thermoreflectance microscopy agreed very well with the FEA results but those obtained using IR thermography did not.

KEY WORDS: MMIC, Power Amplifier, Thermal Modeling, IR thermography, Thermoreflectance.

NOMENCLATURE

CF	Infrared temperature correction factor
T	Temperature, K
a	distance of heat source from base of die, m
b	thickness of die, m
d	distance of heat source from center of die, m
k	Thermal Conductivity, W/mK
l	length of heat source, m

Greek symbols

α	constant
λ	strength of heat source per unit length, W/m

Subscripts

avg	average
j	junction
o	base of substrate

INTRODUCTION

Getting the heat out of devices or systems is one of the challenges of electronics design as the drive for ever lower "on-resistance" in power FETs has reached a plateau (the new constraint is package power/heat dissipation). It is also this aspect that potentially affects reliability the most, as many integrated circuit (IC) packaging failure mechanisms have been found to be dependent upon temperature gradients, magnitude of temperature cycles, rate of temperature change, and absolute temperature. Therefore, temperature must be controlled to meet both performance and reliability requirements.

While detailed temperature or temperature gradients on a die/device can be difficult to measure experimentally, numerical analysis can be used to estimate these parameters relatively easily. This requires an understanding of die attach and packaging techniques as well as the device geometry and layout. While convective and radiative heat transfers are present when the devices are used with an ultimate heat sink in actual applications, heat transfer by conduction is dominant at the individual device level. Hence, convection and radiation heat loss at the surface of the MMIC chip will be neglected.

To correctly obtain the junction or gate temperature of the MMIC chip, accurate thermal modeling of the power amplifier MMIC is required. Commercial thermal simulators such as ANSYS and Abaqus, which are based on Finite Element Analysis (FEA), can be used to solve for temperature distributions in MMICs. However, it is usually very difficult to obtain accurate values for the gate temperatures as the gates are usually submicron in size, while the devices are usually a few millimeters in size. A proper modeling technique and a tool that can simultaneously handle high mesh transitions, temperature dependent and anisotropic thermal properties is required. There are many publications [1-8] related to MMIC thermal modelling and analysis to understand their methodologies, modelling schemes, their rationales for adopting such schemes, as well as the "accuracy" of such schemes when compared with available measured data. Special focus was also placed on determining how the heat dissipation regions in the gates were modelled by various authors. From these studies, it was concluded that volumetric heat source model is more accurate as it is less sensitive to changes in size and depth of heat dissipation region as compared to planar heat sources. Uncertainty in the heat dissipation region raises the need of consistent definition of heat source regions so that temperature prediction from the thermal model can be related to actual application.

In this paper, a detailed metal-layer stack-up configuration for accurate representation of an actual power amplifier MMIC will be presented. To verify our thermal model, the gate temperature of the MMIC was measured using IR thermography and thermoreflectance thermography and compared with that calculated using FEA. In order to reduce the effort required to represent the detailed geometry of the MMIC for the FEA, a simpler model was tried and found to give results which are close to that obtained with all the detailed geometric features modeled.

DESCRIPTION OF THE POWER AMPLIFIER MMIC

The device chosen for this study is a power amplifier (PA) MMIC fabricated in the Microsystems Technology Design Centre of Temasek Labs@NTU. The amplifier is a single stage power amplifier consisting of two 10 x 150µm transistors (Fig. 1) and is capable of providing 1W of output power. The power amplifier MMIC was soldered onto a Cu-Mo carrier with Au-Sn solder and assembled into an aluminium jig (Fig. 2) for thermal characterisation using IR and thermoreflectance thermography.

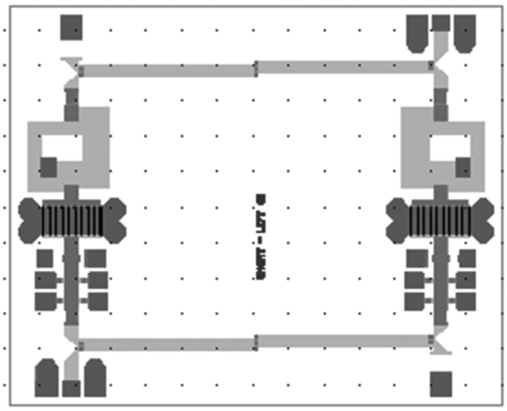

Fig. 1. Layout of the PA MMIC with two 10 x 150µm gates.

MODELING METHODOLOGY

Detailed Thermal Modeling of PA MMIC

The actual dimensions of the carrier and the aluminium jig were modelled (Fig. 3). Established thermal conductivity values (both isotropic and anisotropic), tabulated in Table 1, were used in the thermal model. All thermal conductivities were assumed to be constant except for that of GaAs which was assumed to vary with temperature. The thermal contact/interface resistance between the Cu-Mo carrier and the aluminium jig was set at 193 K-mm^2/W which was empirically determined by Decker and Rosata in [9] and [10] . The thermal analyses of this detailed model were conducted with the aluminium jig base (or bottom surface) temperature set at some specified temperature depending on the experimental conditions.

The metal-layer stack-up configuration used during the fabrication of the power amplifier MMIC is shown in Fig. 4. This same material stack-up configuration has been modeled in a detailed thermal model of the power amplifier MMIC chip.

As indicated in Fig. 4, the heat dissipated by each transistor is modeled as a uniform volumetric heat source (VHS). This VHS region for each of the transistors has the same width and length dimension as the gate and, has a height of 0.28µm, and is located 0.28µm below the top surface of the mesa as shown in Fig. 4 [2].

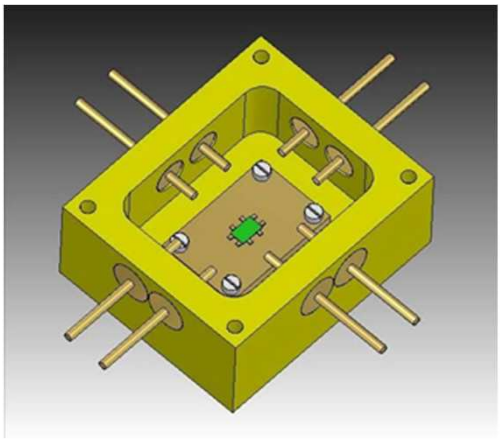

Fig. 2. Assembly of PA MMIC into the aluminium jig

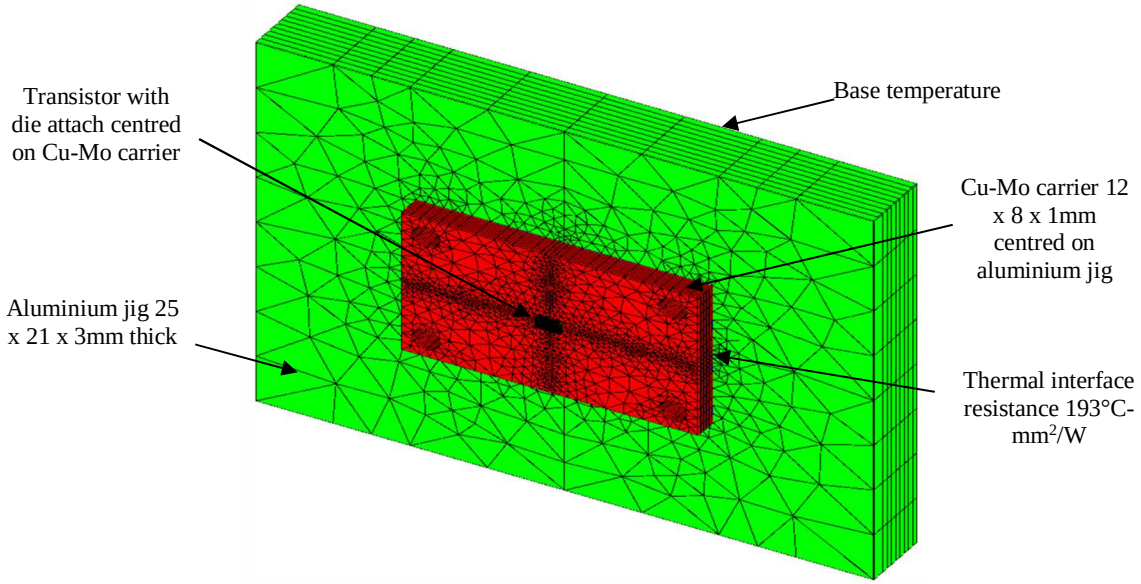

Fig. 3 Three dimensional thermal model of "packaged" PA MMIC .

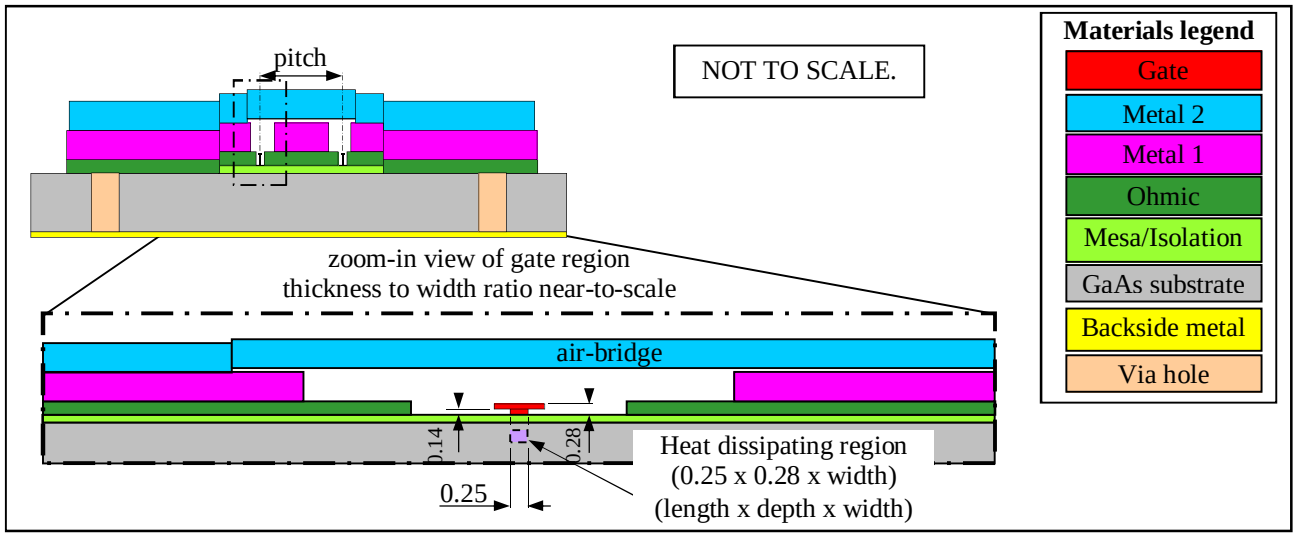

Fig. 4. Cross-sectional view of metal layer build-up in transistors and critical geometric parameters.

Table 1. Thermal conductivity of materials.

Materials/Features	**Thermal conductivity (W/m-K)**	
	in-plane	**through-thickness**
Gate stem, cap and pad	252.0	90.6
Metal 2 or top metal	315.0	
Air-bridge and pillar	315.0	
Metal 1 or 1st metal	259.8	110.2
Ohmic metal	279.5	192.9
Isolation/Mesa – GaAs	$56968.5 * T^{-1.23}$	
Substrate – GaAs	$56968.5 * T^{-1.23}$	
Backside metallization	315.0	
Via Hole – filled gold	315.0	
Die Attach – 80/20 AuSn	57.12	
Carrier - 85/15 Cu-Mo	166.2	
Aluminum – 6061-T6	167.5	

Simplified Thermal Modeling of PA MMIC

While the detailed thermal model should yield more accurate results, it requires a great deal of effort and time to model the metal layers and air bridges of complex geometries around the gate region. Hence, a simplified model which is much easier to model and analyze was developed and its accuracy is compared with the detailed model in this study. In the simplified model, the metal-layer stack-up configuration is ignored. Only five component parts were modeled, namely the gate, GaAs substrate, Au-Sn solder, Cu-Mo carrier and the aluminum jig (Fig. 5). The actual dimensions and material property of each part are the same as the detailed model shown in Fig. 4 and Table 1, respectively. A mesh element size of 0.25µm was used around the gates with a mesh transition to 25µm at the edge of substrate.

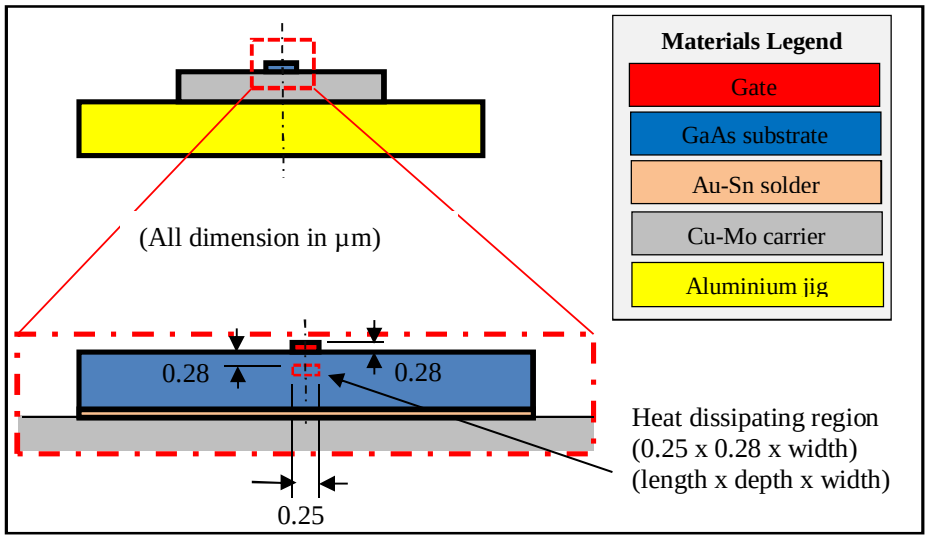

Fig. 5. Cross-sectional view of a simplified thermal model of the PA MMIC.

THERMOREFLECTANCE THERMOGRAPHY

Measurement Methodology

Thermoreflectance, which has a spatial resolution of 0.2 to 0.5µm and fast acquisition time, is good for temperature characterization of reflective surfaces present on most semiconductor devices. It is based on the measurement of relative change in reflectivity of a sample surface as a function of change in temperature. In this work, a 50X objective lens was used such that the spatial resolution was 0.232µm.

IR THERMOGRAPHY

Measurement Methodology

To measure the temperature distribution on the top surface of the MMIC chip, a mid-wavelength (3µm to 5µm) CEDIP infrared camera was used. Its spatial resolution is 5µm. An IR camera actually measures the radiance of an object, and not directly its temperature. The radiance of an object is measured by the detector in the camera and is converted to temperature readings by a software which takes into account the emissivity of the surface. If the emissivity varies over the surface, as it does in this case, an emissivity map has to be taken prior to the measurement of the actual temperature distribution using the IR camera.

Inferring Gate Temperature from IR Thermal Map

The 5µm spatial resolution of the CEDIP IR camera used is much larger than the 0.25µm gate length of the power amplifier MMIC. Consequently, the peak operating junction temperature, T_j, at the gate cannot be directly read from the thermal map typically obtained by the IR camera. The apparent temperature of a pixel of the thermal map is actually an average value, T_{avg}, of the temperature distribution over the pixel. The peak temperature within a pixel can be inferred if the profile of the temperature distribution over the pixel is known. To obtain this profile, an analytical solution of the temperature distribution for a line heat source of finite length l (Fig. 6) in a semi-finite slab of constant thermal conductivity was obtained and given in eqn. (1).

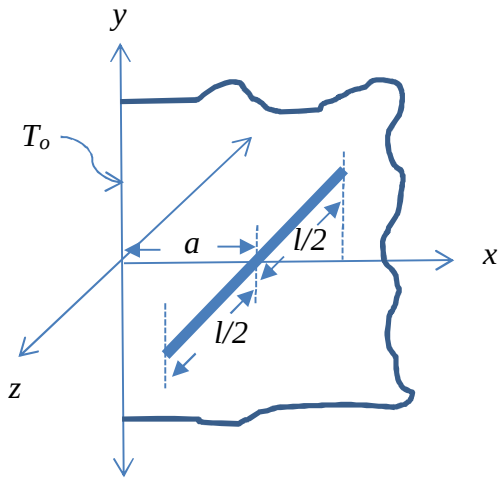

Fig. 6 Line heat source of finite length l in a semi-finite slab.

$$T_1(x,y,z) = \left[T_o^{1-\alpha} + \frac{(1-\alpha)}{T_o^{\alpha}} \frac{\lambda}{4\pi k(T_o)} \theta\right]^{\frac{1}{1-\alpha}} \quad (1)$$

where

$$\theta = \ell n \left\{ \frac{\left[(z+0.5)+\sqrt{(x-a)^2+y^2+(z+0.5)^2}\right]}{\left[(z-0.5)+\sqrt{(x-a)^2+y^2+(z-0.5)^2}\right]} \cdot \frac{\left[(z-0.5)+\sqrt{(x+a)^2+y^2+(z-0.5)^2}\right]}{\left[(z+0.5)+\sqrt{(x+a)^2+y^2+(z+0.5)^2}\right]} \right\} \quad (2)$$

and T_o is the temperature of the base of the substrate. Kirchhoff's transformation was used to account for the temperature dependent thermal conductivity k where

$$k = K\left(T_{ref} / T\right)^{\alpha} \quad (3)$$

where K = 51 W/mK, T_{ref} = 300 K and α = 1.23 for GaAs. Using a mirror imaging technique and transforming coordinates, the temperature distribution due to a single line heat source in a die (Fig. 7) can be calculated from eqn. (4):

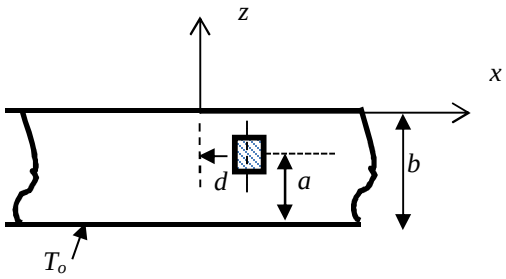

Fig. 7. Heat source of length l in substrate of thickness b.

$$T(x,y,z) = T_1(b+z, x-d, y) + T_1(b-z, x-d, y) \quad (4)$$

where d is the distance of the heat source away from the center of the die (Fig. 7).

It is noted that T_o in eqn. (1) is assumed to be constant over the base of the substrate. However, as can be observed from the FEA results, the temperature along the base of the substrate does vary slightly. Hence the value of T_o used in eqn. (1) is the average temperature of the base of the substrate calculated from the FEA results.

For multi heat sources in a die, the temperature distribution can be calculated by superposition of eqn. (4).

To obtain the true junction temperature, T_j, from the pixel-averaged temperature, T_{avg}, values measured by the IR camera, an Infrared Correction Factor, CF_{IR}, is used where:

$$CF_{IR} = T_j / T_{avg} \quad (5)$$

T_j can be calculated using eqn. (1) and T_{avg} in a pixel can be calculated from eqn. (6) below:

$$T_{avg} = \frac{1}{pixel\ area}\left[T_j \times 2rL_g + 4r\int_{\frac{L_g}{2}}^{r} T dx\right] \quad (6)$$

All experimental values of gate temperature were "corrected" using CF_{IR} to obtain the true peak junction temperature.

COMPARISON OF NUMERICAL AND EXPERIMENTAL RESULTS

Assuming a temperature of 25°C at the base of the aluminum jig, the temperature distribution in the MMIC was calculated using FEA of the detailed and simplified thermal models. As can be seen in Fig. 8, the maximum gate temperatures obtained using the simplified thermal model is higher than that obtained using the detailed model by about 5°C/W. This result is expected due to the presence of metal-layers in the detailed model which helped to facilitate heat spreading and lead to lower surface temperatures,. Therefore, while the detailed model may predict a temperature distribution that is closer to reality, the simplified model which is easier to implement, gives a temperature which is only slightly greater than the actual.

The values of the maximum junction (also called gate) temperature of the MMIC measured using thermoreflectance thermography [11] are plotted in Fig. 8 for comparison with the numerical values calculated using the detailed and simplified thermal models. It can be seen that the experimental measurements using thermoreflectance thermography agree very well with the finite element solutions.

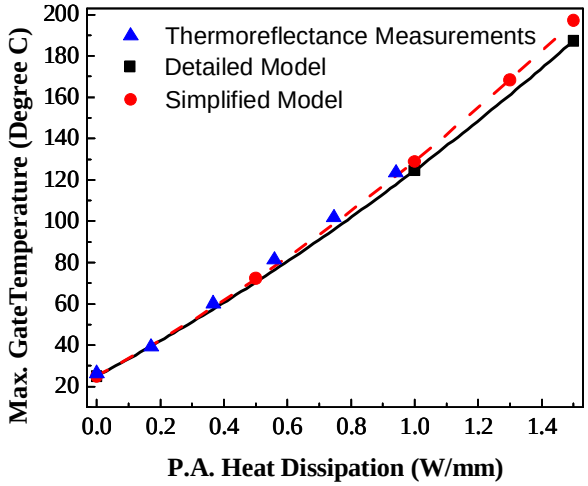

Fig. 8 Numerical and measured temperatures using thermoreflectance thermography for a 24µm-gate pitch PA MMIC.

The results of the simplified thermal model will now be compared with the experimental measurements using IR thermography. Fig. 9 shows a typical emissivity map of the power amplifier MMIC under study. Positions of the ten gates, spaced at 24µm apart can be clearly discerned from the line-scan that shows the emissivity distribution along a line drawn through the mid-width of the gates.

Fig. 10 shows a typical "live" IR image of the power amplifier MMIC. Temperature and positions of the ten gates can be discerned from the line-scan that shows the temperature distribution along a line drawn through the mid-width of the gates.

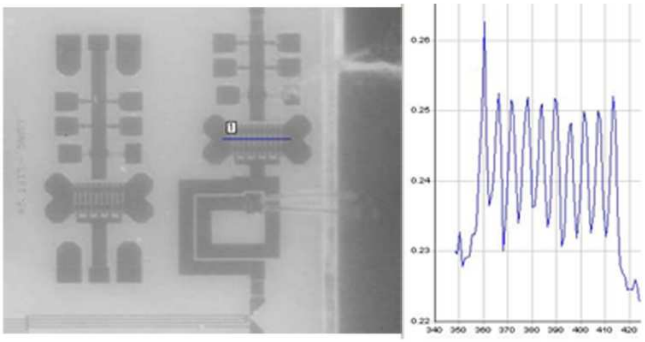

Fig. 9 Emissivity map of the DC biased PA MMIC.

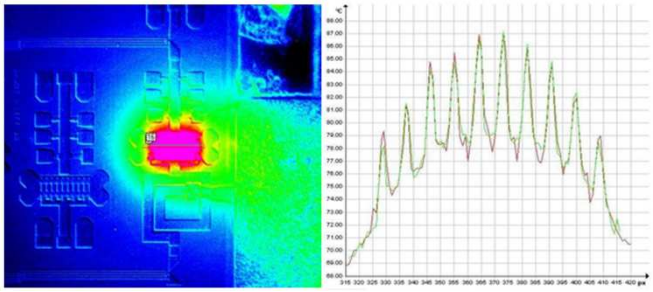

Fig. 10 "Live" IR image of the DC biased PA MMIC.

Temperatures measured using IR thermography and "corrected" using CF_{IR} from eqn. (5) to obtain the true peak operating junction temperatures are plotted in Fig. 11, together with peak junction temperatures calculated using the simplified thermal model. Due to heating from the transistors, the base temperature of the aluminium jig increased as power input increased. The temperature of the base of the aluminium jig measured using a thermocouple was used as a boundary condition in the FEA of the simplified thermal model.

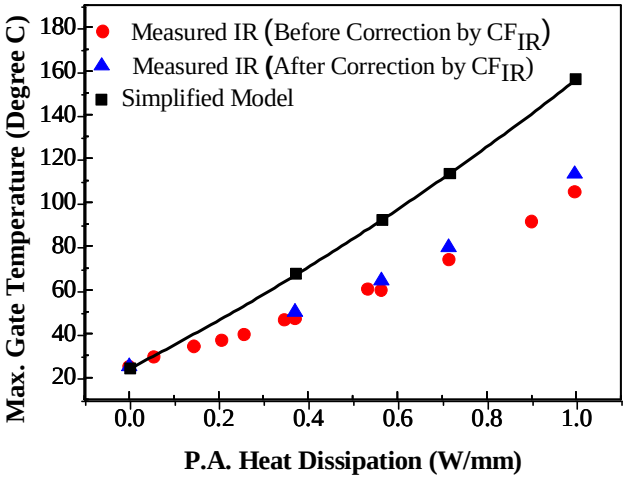

Fig. 11 Numerical and corrected IR- measured temperatures for a 24µm-gate pitch PA MMIC.

As can be seen from Fig. 11, most of the measured temperatures are much lower than those calculated using FEA.

The differences between the modelled and measured IR results could be due to many factors, including:

- Errors in the IR temperature measurements may have caused some discrepancy. For example, reflected background radiation from surrounding parts of the structure may have induced errors in the measurements. Similarly, interfering IR radiation from other metallised areas could also distort the measured surface temperature profile.
- Low emissivity surfaces pose a challenge to obtaining accurate IR measurements.

It can be seen that both calculated and measured temperatures showed more rapid rise with increasing power due to the reduction in thermal conductivity of GaAs at higher temperatures.

CONCLUSION

A detailed and a simplified finite element thermal model have been developed for two MMIC chips. It was shown that the maximum junction temperature obtained using the simplified model higher than that obtained using the detailed model by about 2ºC/W to 5ºC/W, i.e. 2% to 4% difference. The maximum junction temperature obtained from FEA model correlates well with Thermoreflectance measurements. Measured temperature using Infrared thermography is "corrected" using Infrared Correction Factor CF_{IR} due to insufficient of spatial resolution and is compared with a simplified finite element thermal model. The model and "corrected" measurement shows large discrepancy which could be attributed to errors due to reflections and emissivity of PA MMIC surface.

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